PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 :
G11C 5/14, 8/00, 11/408

A1

(11) International Publication Number: **WO 00/10171**

(43) International Publication Date: 24 February 2000 (24.02.00)

(21) International Application Number: PCT/US99/18536

(22) International Filing Date: 13 August 1999 (13.08.99)

(30) Priority Data:
09/134,488 14 August 1998 (14.08.98) US
09/332,757 14 June 1999 (14.06.99) US

(71) Applicant: MONOLITHIC SYSTEM TECHNOLOGY, INC. [US/US]; 1020 Stewart Drive, Sunnyvale, CA 94086–3914 (US).

(72) Inventors: LEUNG, Wingyu; 10450 Orange Avenue, Cupertino, CA 95014–2825 (US). HSU, Fu–Chieh; 21775 Congress Hall Lane, Saratoga, CA 95070–9714 (US).

(74) Agent: HOFFMAN, E., Eric; Bever & Hoffman, LLP, Suite 320, 2099 Gateway Place, San Jose, CA 95110–1017 (US).

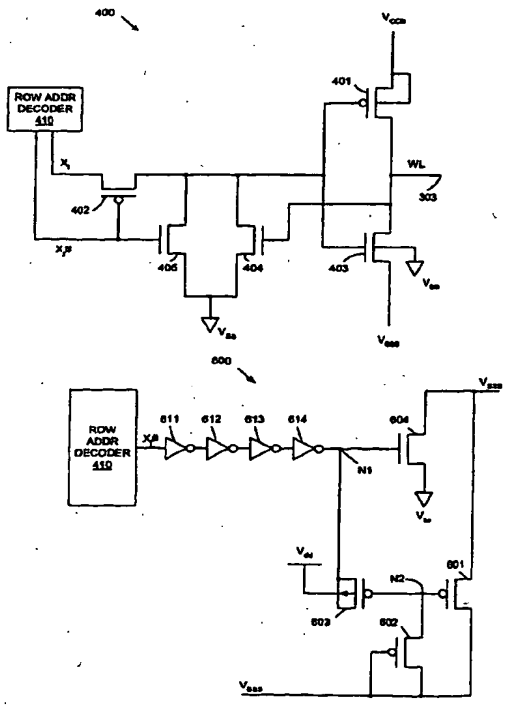
(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: ON–CHIP WORD LINE VOLTAGE GENERATION FOR DRAM EMBEDDED IN LOGIC PROCESS

(57) Abstract

A memory system that includes a dynamic random access memory (DRAM) cell (300), a word line (303), and a CMOS word line driver (400) fabricated using a conventional logic process. The word line driver (400) is controlled to provide a positive boosted voltage and a negative boosted voltage to the word line (303), thereby controlling access to the DRAM cell (300). A positive boosted voltage generator (700) is provided to generate the positive boosted voltage, such that this voltage is greater then V_{dd} but less than V_{dd} plus the absolute value of a transistor threshold voltage V_t. Similarly, a negative boosted voltage generator (800) is provided to generate a negative boosted voltage, such that this voltage is less than V_{ss} by an amount less than V_t. A coupling circuit (600) is provided between the word line driver (400) and one of the positive or negative boosted voltage generators (700 or 800). The coupling circuit (600) couples the word line driver (400) to the selected one of the positive or negative boosted word line generators only when the word line (303) is activated. The positive boosted voltage generator (700) includes a charge pump control circuit (1000) that limits the positive boosted voltage to a voltage less than V^{dd} plus V_t. Similarly, the negative boosted voltage generator (800) includes a charge pump control circuit (1100) that limits the negative boosted voltage to a voltage greater than V_{ss} minus V_t.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

ON-CHIP WORD LINE VOLTAGE GENERATION FOR DRAM EMBEDDED IN LOGIC PROCESS

Wingyu Leung
Fu-Chieh Hsu

RELATED APPLICATIONS

The present application is a continuation-in-part of commonly owned co-pending U.S. Patent Application Serial No. 09/134,488, "Memory Cell For DRAM Embedded in Logic" by Wingyu Leung and Fu-Chieh Hsu, filed August 14, 1998.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to Dynamic Random Accessible Memory (DRAM). More particularly, this invention relates to DRAM fabricated using a conventional logic process. This invention further relates to the on-chip generation of precision voltages for the operation of DRAM embedded or fabricated using a conventional logic process.

Related Art

Fig. 1A is a schematic diagram of a conventional DRAM cell 100 that is fabricated using a conventional logic process. Fig. 1B is a cross sectional view of DRAM cell 100. As used herein, a conventional logic process is defined as a semiconductor fabrication process that uses only one layer of polysilicon and provides for either a single-well or twin-well structure. DRAM cell 100 consists of a p-channel MOS access transistor 1 having a gate terminal 9 connected to word line 3, a drain terminal 17 connected to bit line 5, and a source terminal 18 connected to the gate 11 of a p-channel MOS transistor 2. P-channel transistor 2 is configured to operate as a charge storage capacitor. The source and drain 19 of transistor 2 are commonly connected. The source, drain

and channel of transistor 2 are connected to receive a fixed plate bias voltage V_{pp}. The V_{pp} voltage is a positive boosted voltage that is higher than the positive supply voltage V_{dd} by more than a transistor threshold voltage V_t.

As used herein, the electrode of the charge storage capacitor is defined as the node coupled to the access transistor, and the counter-electrode of the charge storage capacitor is defined as the node coupled to receive a fixed plate bias voltage. Thus, in DRAM cell 100, the gate 11 of transistor 2 forms the electrode of the charge storage capacitor, and the channel region of transistor 2 forms the counter-electrode of the charge storage capacitor.

To improve soft-error-rate sensitivity of DRAM cell 100, the cell is fabricated in an n-well region 14 which is located in a p-type substrate 8. To minimize the sub-threshold leakage of access transistor 1, n-well 14 is biased at the V_{pp} voltage (at n-type contact region 21). However, such a well bias increases the junction leakage. As a result, the bias voltage of n-well 14 is selected such that the sub-threshold leakage is reduced without significantly increasing the junction leakage. When storing charge in the storage capacitor, bit line 5 is brought to the appropriate level (i.e., V_{dd} or V_{ss}) and word line 3 is activated to turn on access transistor 1. As a result, the electrode of the storage capacitor is charged. To maximize the stored charge, word line 3 is required to be driven to a negative boosted voltage V_{bb} that is lower than the supply voltage V_{ss} minus the absolute value of the threshold voltage (V_{tp}) of access transistor 1.

In the data retention state, access transistor 1 is turned off by driving word line 3 to the V_{dd} supply voltage. To maximize the charge storage of the capacitor, the counter electrode is biased at the positive boosted voltage V_{pp}. The plate voltage V_{pp} is limited by the oxide

breakdown voltage of the transistor 2 forming the charge storage capacitor.

DRAM cell 100 and its variations are documented in U.S. Patent No. 5,600,598, entitled "Memory Cell and Wordline Driver For Embedded DRAM in ASIC Process," by K. Skjaveland, R. Township, P. Gillingham (hereinafter referred to as "Skjaveland et al."), and "A 768k Embedded DRAM for 1.244Gb.s ATM Switch in a 0.8um Logic Process," P. Gillingham, B. Hold, I. Mes, C. O'Connell, P. Schofield, K. Skjaveland, R. Torrance, T. Wojcicki, H. Chow, Digest of ISSCC, 1996, pp. 262-263 (hereinafter referred to as "Gillingham et al.). Both Skjaveland et al. and Gillingham et al. describe memory cells that are contained in an n-well formed in a p-type substrate.

Fig. 2 is a schematic diagram of a word line control circuit 200 including a word line driver circuit 201 and a word line boost generator 202 described by Gillingham et al.. Word line control circuit 200 includes p-channel transistors 211-217, inverters 221-229, NAND gates 231-232 and NOR gate 241, which are connected as illustrated. Word line driver 201 includes p-channel pull up transistor 211, which enables an associated word line to be pulled up to the V_{dd} supply voltage. P-channel pull down transistors 212-217 are provided so that the word line can be boosted down to a negative voltage (i.e., -1.5V) substantially below the negative supply voltage V_{ss}. However, the p-channel pull down transistors 212-217 have a drive capability much smaller (approximately half) than an NMOS transistor of similar size. As a result, the word line turn on of Gillingham et al. is relatively slow (>10ns). Furthermore, in the data retention state, word line driver 201 only drives the word line to the V_{dd} supply voltage. As a result, the sub-threshold leakage of the access transistor in the memory cells may not be adequately suppressed.

DRAM cells similar to DRAM cell 100 have also been formed using n-channel transistors fabricated in a p-type well region. To maximize stored charge in such n-channel DRAM cells during memory cell access, the associated word line is driven to a voltage higher than the supply voltage V_{dd} plus the absolute value of the threshold voltage (V_{tn}) of the access transistor. In the data retention state, the n-channel access transistor is turned off by driving the word line to V_{ss} supply voltage (0 Volts). To maximize the charge storage of the capacitor in an n-channel DRAM cell, the counter electrode is biased at a plate voltage V_{bb} that is lower than the V_{ss} supply voltage.

A prior art scheme using n-channel DRAM cells includes the one described by Hashimoto et al. in "An Embedded DRAM Module using a Dual Sense Amplifier Architecture in a Logic Process", 1997 IEEE International Solid-State Circuits Conference, pp. 64-65 and 431. A p-type substrate is used, such that the memory cells are directly in contact with the substrate and are not isolated by any well structure. In the described design, substrate bias is not permitted. Moreover, application of a negative voltage to the word line is not applicable to ASICs that restrict substrate biasing to be zero. Consequently, the architecture achieves a negative gate-to-source voltage (V_{gs}) by limiting bit line swing. The negative V_{gs} voltage reduces sub-threshold leakage in the memory cells. Hashimoto et al. fails to describe the structure of the word line driver.

It would therefore be desirable to have a word line driver circuit that improves the leakage currents in DRAM cells fabricated using a conventional logic process. Moreover, it would be desirable to have improved methods for biasing DRAM cells fabricated using a conventional logic process.

SUMMARY

Accordingly, the present invention provides a memory system that includes a dynamic random access memory (DRAM) cell, a word line, and a CMOS word line driver fabricated using a conventional logic process. The word line driver is controlled to selectively provide a positive boosted voltage and a negative boosted voltage to the word line, thereby controlling access to the DRAM cell.

A positive boosted voltage generator is provided to generate the positive boosted voltage, such that the positive boosted voltage is greater than the V_{dd} supply voltage but less than the V_{dd} supply voltage plus the absolute value of a transistor threshold voltage V_t.

Similarly, a negative boosted voltage generator is provided to generate the negative boosted voltage, such that the negative boosted voltage is less than the V_{ss} supply voltage, but greater than the V_{ss} supply voltage minus the absolute value of a transistor threshold voltage V_t.

A coupling circuit is provided between the word line driver and one of the positive or negative boosted voltage generators. For example, if the DRAM cell is constructed from PMOS transistors, then the coupling circuit couples the word line driver to the negative boosted word line generator. When the DRAM cell is being accessed, the coupling circuit couples the word line driver to the negative boosted voltage, thereby turning on the p-channel access transistor of the DRAM cell. However, when the DRAM cell is not being accessed, the coupling circuit couples the word line driver to the V_{ss} supply voltage, thereby minimizing leakage currents associated with the negative boosted voltage.

In this embodiment, the coupling circuit can be configured to provide the V_{ss} supply voltage to the word line driver when the word line is first activated. When the voltage on the word line falls below the V_{dd} supply

voltage, the coupling circuit provides the negative boosted voltage to the word line driver.

Conversely, if the DRAM cell is constructed from NMOS transistors, then the coupling circuit couples the word line driver to the positive boosted word line generator. When the DRAM cell is being accessed, the coupling circuit couples the word line driver to the positive boosted voltage, thereby turning on the n-channel access transistor of the DRAM cell. However, when the DRAM cell is not being accessed, the coupling circuit couples the word line driver to the V_{dd} supply voltage, thereby minimizing leakage currents associated with the positive boosted voltage.

In this embodiment, the coupling circuit can be configured to provide the V_{dd} supply voltage to the word line driver when the word line is first activated. When the voltage on the word line rises above the V_{ss} supply voltage, the coupling circuit provides the positive boosted voltage to the word line driver.

The positive boosted voltage generator includes a charge pump control circuit that limits the positive boosted voltage to a voltage less than V_{dd} plus V_t. Similarly, the negative boosted voltage generator includes a charge pump control circuit that limits the negative boosted voltage to a voltage greater than V_{ss} minus V_t. The positive and negative boosted voltages are limited in this manner because, for normal logic applications using sub 0.25 micron processes, the gate oxide breakdown voltage is usually less than a threshold voltage V_t above the positive supply voltage V_{dd}.

The positive boosted voltage generator includes a charge pump control circuit that limits the positive boosted voltage to a voltage that is greater than the V_{dd} supply voltage by less than one transistor threshold voltage. In one embodiment, this charge pump control circuit includes a first p-channel transistor having a

source coupled to the V_{dd} supply voltage and a drain coupled to a first reference current source. The gate of the first p-channel transistor is coupled to the gate of a second p-channel transistor. The first and second p-channel transistors have first and second channel widths, respectively, wherein the second channel width is greater than the first channel width. A second reference current source is coupled to the drain of the second p-channel transistor. The drain of the second p-channel transistor provides an inhibit control signal for the charge pump control circuit. A third p-channel transistor has a gate and a drain connected to a source of the second p-channel transistor, and a source coupled to receive the positive boosted voltage. The ratio of the first and second channel widths is selected such that the inhibit control signal is asserted when positive boosted voltage is less than one transistor threshold voltage greater than the V_{dd} supply voltage. In one embodiment, the first reference current source has a negative temperature coefficient to compensate for temperature effects of the second p-channel transistor. The second reference current source can be provided with a positive temperature coefficient to compensate for temperature effects of the third p-channel transistor.

Similarly, the negative boosted voltage generator includes a charge pump control circuit that limits the negative boosted voltage to a voltage that is less than the V_{ss} supply voltage by less than one transistor threshold voltage V_t. In one embodiment, this charge pump control circuit includes a first n-channel transistor having a source coupled to the V_{ss} supply voltage and a drain coupled to a first reference current source. The gate of the first n-channel transistor is coupled to the gate of a second n-channel transistor. The first and second n-channel transistors have first and second channel widths, respectively, wherein the second channel width is

greater than the first channel width. A second reference current source is coupled to the drain of the second n-channel transistor. The drain of the second n-channel transistor provides an inhibit control signal for the charge pump control circuit. A p-channel transistor has a source coupled to the source of the second n-channel transistor, and a drain and gate coupled to receive the negative boosted voltage. The ratio of the first and second channel widths is selected such that the inhibit control signal is asserted when negative boosted voltage is greater than the V_{ss} supply voltage minus the absolute value of a transistor threshold voltage V_t. In one embodiment, the first reference current source has a negative temperature coefficient to compensate for temperature effects of the second n-channel transistor. The second reference current source can be provided with a positive temperature coefficient to compensate for temperature effects of the p-channel transistor.

The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a schematic diagram of a conventional DRAM memory cell formed by p-channel MOS transistors fabricated using a conventional logic process.

Fig. 1B is a cross sectional diagram of the DRAM memory cell of Fig. 1A.

Fig. 2 is a schematic diagram of a conventional word line control circuit, including a word line driver and a word line voltage generator.

Fig. 3A is a schematic diagram of a DRAM memory cell that is supplied by voltage sources in accordance with one embodiment of the present invention.

Fig. 3B is a cross sectional view of the DRAM memory cell of Fig. 3A.

Fig. 3C is a layout view of the DRAM memory cell of Fig. 3A in accordance with one embodiment of the present invention.

Fig. 3D is a cross sectional view of the DRAM memory cell of Fig. 3A in accordance with another embodiment of the present invention.

Fig. 4 is a schematic diagram of a word line driver in accordance with one embodiment of the present invention.

Fig. 5 is a block diagram illustrating a word line driver system that includes a first plurality of word line drivers, a second plurality of V_{SSB} coupling circuits, a V_{CCB} voltage generator and a V_{BBS} voltage generator in accordance with one embodiment of the present invention.

Fig. 6 is a schematic diagram of a V_{SSB} coupling circuit in accordance with one embodiment of the present invention.

Fig. 7 is a waveform diagram illustrating various signals generated during the operation of the V_{SSB} coupling circuit of Fig. 6.

Fig. 8 is a block diagram of V_{CCB} and V_{SSB} boosted voltage generators in accordance with one embodiment of the present invention.

Fig. 9A is a simplified schematic diagram of a charge pump control circuit used in a conventional positive boosted voltage generator.

Fig. 9B is a simplified schematic diagram of a charge pump control circuit used in a conventional negative boosted voltage generator.

Fig. 10 is a schematic diagram of a V_{CCB} charge pump control circuit in accordance with the one embodiment of the present invention.

Fig. 11 is a schematic diagram of a V_{BBS} charge pump control circuit in accordance with the one embodiment of the present invention.

Figs. 12-17 are schematic diagrams of reference current sources in accordance with various embodiments of the present invention.

Fig. 18 is a schematic diagram of a word line driver and a V_{BBC} voltage coupling circuit in accordance with an embodiment of the present invention that uses NMOS transistors to form the DRAM cells.

DETAILED DESCRIPTION

The following describes the voltages and biasing of a DRAM memory fabricated using a conventional logic process which is a single or twin well process with a single polycrystalline silicon layer and one or more layers of metal. In the described examples, the positive supply voltage is designated as supply voltage V_{dd}. In general, the positive supply voltage V_{dd} can have a nominal value such as 3.3 Volts, 2.5 Volts, 1.8 Volts, etc., depending on the fabrication process. The ground supply voltage, having a nominal value of 0 Volts, is designated as supply voltage V_{SS}.

As shown in Fig. 3A, a DRAM memory cell used in the described embodiments consists of a p-channel access transistor 301 and a p-channel storage transistor 302 that is configured as a storage capacitor. The gate of the access transistor 301 is connected to word line 303 and the drain of access transistor 301 is connected to bit line 305. The source of access transistor 301 is coupled to the source region of transistor 302. In the described embodiment, only the source region of transistor 302 is actually formed (i.e., there is no drain region of transistor 302). In another embodiment, both the source and drain regions are formed, and these regions are commonly connected to the source of access transistor 301. The channel of transistor 302 forms the electrode of the storage capacitor, and the gate of transistor 302 forms the counter-electrode of the storage capacitor. The

channel of storage transistor 302 (i.e., the electrode of the storage capacitor) is coupled to the source of access transistor 301. The gate of transistor 302 (i.e., the counter-electrode of the storage capacitor) is connected to receive a negative boosted bias voltage V_{bb1}. The bias voltage V_{bb1} is limited by the break-down voltage (V_{bd}) of the gate oxide of capacitor 302 and the highest voltage (V_1) stored on the electrode. In general, bias voltage V_{bb1} is set to a voltage that is greater than V_1 minus V_{bd}. In the preferred embodiment, V_1 is equal to the positive supply voltage V_{dd}, and bias voltage V_{bb1} is set to -0.3 Volts.

In general, the bias voltage V_{bb1} is selected to have a magnitude less than one diode voltage drop. That is, the bias voltage V_{bb1} is selected to have a magnitude less than about 0.7 Volts. The negative bias voltage V_{bb1} linearizes the operation of storage capacitor 302 by increasing the capacitance of capacitor 302 when the electrode is charged to the V_{dd} supply voltage. Without the negative plate bias V_{bb1}, the capacitance of capacitor 302 tends to decrease rapidly as the voltage across the capacitor becomes smaller than the threshold voltage of the MOS structure.

As illustrated in Fig. 3B, DRAM memory cell 300 is contained in an n-doped well 304 of a p-type monocrystalline silicon substrate 306. Multiple memory cells can share the same n-well 304. N-well 304 is biased to a boosted positive voltage (V_{pp1}) that is greater than the V_{dd} supply voltage by a voltage that is approximately equal to the absolute value of the threshold voltage (V_{tp}) of p-channel access transistor 301. In addition, the boosted positive voltage V_{pp1} is selected to be lower than the oxide break down voltage of p-channel access transistor 301. N-well 304 is biased by a connection to n-type contact region 315. In the present embodiment, the V_{pp1} voltage is controlled to be approximately 0.3 Volts

greater than the V_{dd} supply voltage (i.e., V_{tp} = 0.3 Volts). Applying the V_{pp1} voltage to n-well 304 decreases the sub-threshold leakage of access transistor 301, and minimizes the possibility of forward biasing the junction between the electrode of capacitor 302 and n-well 304 due to supply noise. However, applying the V_{pp1} voltage to n-well 304 also increases the junction leakage at the electrode of storage capacitor 302, especially at higher voltages.

When data is written to memory cell 300, bit line 305 is coupled to the V_{dd} supply voltage to write a logic zero data value, or to the V_{ss} supply voltage to write a logic one data value. In addition, word line 303 is coupled to receive a word line voltage V_{SSB}, which has a potential of about -0.3 Volts. In accordance with one embodiment, the V_{SSB} voltage level is chosen to be -0.2 Volts to -0.6 Volts, as compared to -1.0 Volts or more negative in a traditional DRAM implementation. Generation of the V_{SSB} voltage is described in more detail below.

When memory cell 300 is in the data retention state, bit line 305 is pre-charged to a voltage of about one half the V_{dd} supply voltage. Sub-threshold leakage of memory cell 300 tends to be higher when bit line 305 or the electrode of capacitor 302 is at a potential close to the V_{dd} supply voltage. This sub-threshold leakage is more severe for sub-micron transistors because of their lower threshold voltages (e.g., V_{tp} = -0.5 Volts). To reduce the sub-threshold leakage during the data retention state, word line 303 is coupled to an internally generated positive boosted voltage (V_{CCB}) which has a potential about 0.3 Volts greater than the V_{dd} supply voltage. In accordance with one embodiment, the V_{CCB} voltage level is chosen to be 0.2 Volts to 0.6 Volts greater than the V_{dd} supply voltage. This is different from the conventional memory cells described above, in which the word line is coupled to the V_{dd} supply voltage during the data retention

state. Generation of the positive boosted voltage V_{CCB} is described in more detail below.

Fig. 3C shows the layout of memory cell 300 in accordance with one embodiment of the present invention. The connection to bit line 305 is shared between two neighboring cells, and the upper plate 313 of capacitor 302 connects two rows of adjacent cells parallel to the wordline. The capacitors of adjacent cells are electrically isolated through field oxide (FOX) region 314, e.g., at the minimum spacing allowed by the design rules. Because capacitor plate 313 is biased at the Vbb1 level to allow the maximum turn-on of the p-channel capacitor, a worse case biasing exists over field oxide (FOX) 314 with maximum leakage current that can flow between neighboring cell storage nodes. To minimize such field leakage current, the capacitor plate 313 is allowed to cross-over field oxide 314 only along diagonal corners of adjacent storage nodes. This forces the possible leakage path between adjacent cells to be 1.414 times the minimum FOX isolation spacing, and at the same time reduces the portion of the storage node perimeter (at minimum spacing) that is adversely gated by the capacitor plate 313 to be less than 25% of the total storage node perimeter (which is the channel region of capacitor 302) and thereby minimizes possible leakage current.

Fig. 3D shows an enlarged cross-section view of p-channel access transistor 301 and p-channel capacitor 302 in accordance with another embodiment of the present invention. In this embodiment, the normal p-type heavy source/drain implant and the source/drain salicidation are excluded from the p-type connecting region 312. This arrangement reduces junction leakage current as well as gate-induced drain leakage (GIDL) that can degrade the charge retention time of the storage node. In a conventional logic process, the formation of a p-channel transistor usually follows the sequence of (i) patterning

and etching the polysilicon gate, (ii) using ion implantation to lightly dope the source/drain regions right at the gate edges, thereby forming p-LDD regions, (iii) forming insulating sidewall spacers, (iv) forming salicide (self-aligned silicide) on the exposed silicon surfaces, and (v) using ion implantation to heavily dope the source/drain regions on the exposed silicon surfaces, thereby forming p-S/D regions. The two-step formation of the p-LDD and p-S/D regions provide for high conduction current and good leakage current control at the same time. The p-S/D region is usually much more heavily doped to have low resistivity than the p-LDD region. As a result, the junction breakdown voltage is lower and leakage current of the p-S/D region is much higher than that of the p-LDD region. The source/drain salicide reduces the source/drain resistivity further but also degrades the junction leakage further. Therefore, it is important to exclude as much heavy p-type doping and salicide formation in the storage node (i.e., region 312) as possible.

In the present invention, region 312 is laid out with minimum polysilicon gate spacing which is comparable to twice the size of the insulating sidewall spacers 325. With this layout arrangement, p-S/D doping and salicide are effectively excluded from region 312 without need for additional processing steps.

The DRAM cell of Figs. 3A-3D may similarly be implemented using an n-channel access transistor and capacitor, provided that these elements are fabricated in a p-doped well located in either an n-doped substrate or in a deep n-doped well of a p-doped substrate.

Fig. 4 is a schematic diagram of a word line driver 400 used to drive word line 303 in accordance with one embodiment of the present invention. Thus, the output voltages supplied by word line driver 400 are provided to word line 303 (Fig. 3A). Word line driver 400 consists of P-channel transistors 401-402 and N-channel transistors

403-405. To deactivate word line 303, transistor 401 is turned on, thereby pulling word line 303 up to the positive boosted word line voltage V_{CCB}. The V_{CCB} word line voltage is high enough to turn off access transistor 301. To activate word line 303, pull-down transistor 403 is turned on, thereby pulling down word line 303 to the V_{SSB} voltage. The generation of the V_{SSB} word line voltage is described in more detail below.

The gate of word line pull-up transistor 401 and the gate of word line pull-down transistor 403 are commonly connected to a pass gate formed by p-channel transistor 402. Transistor 402, when turned on, couples transistors 401 and 402 to receive an output signal X_i provided by a row address decoder 410. The gate of transistor 402 is coupled to receive another output signal X_j# from row address decoder 410. When the memory cells connected to word line 303 are selected for access, row address decoder 410 first drives the X_i signal high, and then drives the X_j# signal low. The low state of the X_j# signal turns on pass transistor 402, which provides the logic high X_i signal to the gates of the pull up and pull down transistors 401 and 403. Under these conditions, pull down transistor 403 is turned on, thereby coupling word line 303 to receive the V_{SSB} word line voltage.

As described in more detail below, row address decoder 410 controls a first subset of word lines that includes word line 303 and a plurality of other word lines. If word line 303 is not selected for access (but another word line in the first subset of word lines is selected for access), then row address decoder 410 provides logic low values for both the X_i and X_j# signals. Under these conditions, the gates of pull up and pull down transistors 401 and 403 are maintained at logic low states by n-channel transistor 404. Note that the gate of transistor 404 is connected to word line 303, which is maintained at a logic high value when word line 303 is not

being accessed. As a result, transistor 404 is turned on when word line 303 is not being accessed, thereby coupling the gates of transistors 401 and 403 to the V_{SS} supply voltage. The V_{SS} supply voltage turns on pull up transistor 401 and turns off pull down transistor 403, thereby maintaining a logic high voltage (i.e., V_{CCB}) on word line 303.

During the data retention state (i.e., when none of the word lines in the first subset of word lines is being accessed), row address decoder 410 drives the X_j# signal high, thereby turning on n-channel transistor 405. Turned on transistor 405 couples the gates of pull up and pull down transistors 401 and 403 to the V_{SS} supply voltage. As a result, pull up transistor 401 is turned on and pull down transistor 403 is turned off. At this time, transistor 401 couples word line 303 to receive the V_{CCB} voltage, thereby turning off access transistor 301 of memory cell 300.

Pull down transistor 403 is selected to be an n-channel transistor to speed up the turn on of word line 303. However, in the present embodiment, the bulk of all n-channel transistors formed are connected to receive the V_{SS} supply voltage. (See, Fig. 3B, which illustrates p-type substrate 306 coupled to receive the V_{SS} supply voltage). As a result, the minimum value of the V_{SSB} control voltage is limited to one diode voltage drop below the V_{SS} supply voltage (i.e., one diode voltage drop below ground). Moreover, each row of memory cells has an associated word line driver. There are usually numerous rows of memory cells (e.g., more than 100) in an embedded memory. As a result of the large number of word line drivers, the reverse junction leakage between the substrate and the sources of the n-channel pull down transistors (such as pull down transistor 403) can be quite substantial. The reverse junction leakage increases exponentially as the V_{SSB} control voltage becomes more

negative. To limit the reverse junction leakage, the word line drivers are divided into groups of 32, with each group being coupled to a common V_{SSB} coupling circuit 500.

Fig. 5 is a block diagram illustrating a word line driver system 500 that includes a first plurality of word line drivers 400, a second plurality of V_{SSB} coupling circuits 600, a V_{CCB} voltage generator 700 and a V_{BBS} voltage generator 800. Each V_{SSB} coupling circuit 500 is coupled to a corresponding group of 32 word line drivers 400. As described in more detail below, when one of the word lines in a group is to be turned on, the corresponding V_{SSB} coupling circuit 500 is controlled to couple the V_{BBS} voltage generator 800 to the corresponding group of 32 word line drivers. As a result, the V_{SSB} coupling circuit routes the negative boosted voltage V_{BBS} generated by the V_{BBS} voltage generator 800 as the V_{SSB} voltage. As described in more detail below, V_{BBS} voltage generator 800 generates a V_{BBS} voltage having a value less than one threshold voltage (V_{tp}) below the V_{SS} supply voltage. When none of the word lines in a group is to be turned on, the corresponding V_{SSB} coupling circuit 500 is controlled to couple the V_{SS} voltage supply to the corresponding group of 32 word line drivers. That is, the V_{SSB} coupling circuit 500 routes the V_{SS} supply voltage as the V_{SSB} voltage.

Because only a subset of the word line drivers 400 is coupled to receive the V_{BBS} voltage at any given time, the reverse junction leakage is substantially reduced. Moreover, by limiting the V_{BBS} voltage to a voltage less than one threshold voltage below the V_{SS} supply voltage, the reverse junction leakage is further reduced.

Fig. 6 is a schematic diagram of V_{SSB} coupling circuit 600 in accordance with one embodiment of the present invention. V_{SSB} coupling circuit 600 includes p-channel transistors 601-603, n-channel transistor 604 and inverters 611-614. P-channel transistor 601 is connected

between the V_{SSB} and V_{BBS} voltage supply lines. The gate of transistor 601 is coupled to node N2. Transistor 602 is connected between node N2 and the V_{BBS} voltage supply line. P-channel transistor 603 is connected as a capacitor, with its source and drain commonly connected to node N1, and its gate connected to node N2. N-channel transistor 604 is connected between the V_{SSB} voltage supply line and the V_{SS} voltage supply terminal. The gate of transistor 604 is connected to node N1. Inverters 611-614 are connected in series, with inverter 611 receiving the X_j# signal from row address decoder 410, and inverter 614 providing the delayed X_j# signal to node N1.

Fig. 7 is a waveform diagram illustrating various signals generated during the operation of V_{SSB} coupling circuit 600.

Prior to activating word line 303, the X_i signal is low and the X_j# signal is high. Under these conditions, the chain of inverters 611-614 provides a logic high signal to node N1, thereby turning on n-channel transistor 604. As a result, the V_{SSB} supply line is maintained at the V_{SS} supply voltage (0 Volts). Also, prior to activating word line 303, the sub-threshold leakage of transistor 602 pulls node N2 to a voltage less than one threshold voltage drop (V_t) above V_{BBS}, thereby preventing transistor 601 from turning on.

As described above in connection with Fig. 4, the X_i signal is driven high and then the X_j# signal is driven low to activate word line 303. Under these conditions, pull down transistor 403 (Fig. 4) of word line driver 400 turns on, thereby coupling word line 303 to the V_{SSB} supply line. Immediately after transistor 403 is turned on, the low state of the X_j# is propagating through the chain of inverters 611-614 and has not reached node N1. During this time, n-channel transistor 604 remains on, coupling the V_{SSB} supply line to receive the V_{SS} supply voltage. Also during this time, the high state of node N1 pulls the

source and drain of capacitor-coupled transistor 603 to a high state. Transistor 602 is connected as an MOS diode with its gate and drain connected to the V_{BBS} supply line. Transistor 602 therefore limits the voltage at node N2 to no more than one threshold voltage (V_t) above the V_{BBS} voltage, or to a potential approximately equal to the V_{SS} supply voltage. Consequently, capacitor 603 is initially charged to a voltage approximately equal to the V_{dd} supply voltage (i.e., the voltage across transistor 603 is approximately equal to V_{dd}).

When the low state of the X_j# signal reaches node N1, transistor 604 is turned off, thereby de-coupling the V_{SSB} voltage supply line from the V_{SS} voltage supply terminal. The low voltage at node N1 also causes capacitor 603 to pull node N2 down to a voltage equal to $-V_{dd}$. The $-V_{dd}$ voltage at node N2 turns on p-channel transistor 601, thereby coupling the V_{SSB} voltage supply line to the V_{BBS} voltage supply line. Note that only 32 word line drivers are coupled to the V_{BBS} voltage supply line (and therefore the V_{BBS} voltage generator 800) at this time. Because a relatively small number of word line drivers are connected to the V_{BBS} supply line, the resulting junction leakage is relatively small.

The on-chip V_{BBS} voltage generator 800 is designed to maintain V_{BBS} at approximately -0.3 Volts below the V_{SS} supply voltage despite the junction leakage. Note that during the activation of word line 303, this word line 303 is initially coupled to receive the V_{SS} supply voltage. When the voltage of word line 303 drops below the V_{dd} supply voltage, then word line 303 is coupled to receive the negative boosted voltage V_{BBS}. This limits the source-to-drain voltage of word line pull down transistor 403 to be less than V_{CCB} minus V_{BBS}, thereby preventing transistor 403 from being exposed to high voltage stress.

To de-activate word line 303, the X_j# signal is driven high by row address decoder 410. In response, pull up

transistor 401 in word line driver 400 is turned on, thereby pulling up word line 303 to the V_{CCB} voltage. In V_{SSB} coupling circuit 600, the high state of the X_j# signal propagates through the delay chain formed by inverters 611-614, thereby providing a high voltage at node N1 which turns on transistor 604. The high voltage at node N1 also couples node N2 to a voltage of about V_{SS}, thereby turning off transistor 601. Under these conditions, the V_{SSB} voltage supply line is coupled to the V_{SS} voltage supply terminal.

Voltage Reference Generation

The V_{CCB} and V_{SSB} voltages are generated by on-chip charge pump circuits in accordance with one embodiment of the present invention. Fig. 8 is a block diagram showing the general construction of the V_{CCB} and V_{SSB} boosted voltage generators 700 and 800 in accordance with one embodiment of the present invention. Each of the V_{CCB} and V_{SSB} boosted voltage generators consists of a ring oscillator 801, a charge pump 802 and a pump controller 803, which controls the operation of the oscillator 801 and thus charge pump 802. Ring oscillator 801 and charge pump 802 are conventional elements that are well documented in references such as U.S. Patent Nos. 5,703,827 and 5,267,201.

Fig. 9A is a simplified schematic diagram of a charge pump control circuit 901 used in a conventional positive boosted voltage generator. Charge pump control circuit 901 includes a p-channel transistor 911 having a gate coupled to receive the V_{dd} supply voltage, a source and bulk coupled to receive the positive boosted voltage V_{boost+}, and a drain coupled to a reference current source 912. The drain of transistor 911 is also connected to the Inhibit control line. Current source 912 can be replaced with a resistor.

When the V_{boost+} voltage is higher than the V_{dd} supply voltage by one threshold voltage (V_{tp}), transistor 911 is turned on. The source current from transistor 911 is compared to the reference current I_{REF} provided by current source 912. As the potential difference between the V_{boost+} and V_{dd} voltages increases, the source current from transistor 911 increases. When the source current is larger than the reference current I_{REF}, the Inhibit control line is coupled to receive the V_{boost+} voltage. The high state of the Inhibit signal disables the ring oscillator 801, thereby shutting down the charge pump 802 and stopping V_{boost+} from going higher. Depending on the magnitude of the reference current I_{REF}, the boosted voltage V_{boost+} can be regulated at a voltage equal to the V_{dd} supply voltage plus one threshold voltage (V_{tp}) or higher. Note that the bulk of transistor 911 is coupled to receive the V_{boost+} voltage so that the source-to-bulk junction of this transistor is not forward biased. However, this connection is possible only when the bulk of transistor 911 is an N-well which can be isolated from the substrate, or when transistor 911 is formed in an n-type substrate that is biased to a voltage equal to or more positive than V_{boost+}.

Fig. 9B is a simplified schematic diagram of a charge pump control circuit 902 used in a conventional negative boosted voltage generator. Charge pump control circuit 902 includes an n-channel transistor 921 having a gate coupled to receive the V_{SS} supply voltage, a source and bulk coupled to receive the negative boosted voltage V_{boost-}, and a drain coupled to a reference current source 922. The drain of transistor 921 is also connected to the Inhibit# control line. Current source 922 can be replaced with a resistor.

When the V_{boost-} voltage is lower than the V_{SS} supply voltage by one threshold voltage (V_{tn}), transistor 921 is turned on. The drain current from transistor 921 is

compared to the reference current I_{REF} provided by current source 922. As the potential difference between V_{boost-} and V_{SS} increases, the drain current from transistor 921 increases. When the drain current is larger than the reference current I_{REF}, the Inhibit# control line is coupled to receive the V_{boost-} voltage. The low state of the Inhibit# signal disables the ring oscillator 801, thereby shutting down the charge pump 802 and stopping the V_{boost-} voltage from going more negative. Depending on the magnitude of the reference current I_{REF}, the V_{boost-} voltage can be regulated at a voltage equal to V_{SS} minus one threshold voltage (V_{tn}) or more. Note that the bulk of transistor 921 is coupled to receive the V_{boost-} voltage so that the source-to-bulk junction of this transistor is not forward biased. This connection is possible only when the bulk of transistor 921 is a p-well which can be isolated from the substrate, or when transistor 921 is formed in a p-type substrate that is biased a voltage equal to or more negative than V_{boost-}.

Charge pump control circuits 901 and 902 cannot co-exist in a conventional logic process because such a process has the limitation that only one type of transistor can be isolated in a well. That is, both n-wells and p-wells are not available in a conventional logic process as defined herein. Moreover, because the p-type substrate of memory cell 300 is biased at the V_{SS} voltage (Fig. 3B), the p-type substrate of memory cell 300 cannot be biased at a voltage equal to or more negative than the negative boosted word line voltage V_{BBS}. Furthermore, because charge pump control circuit 901 results in a V_{boost+} voltage greater than or equal to V_{dd} plus V_{tp}, this charge pump control circuit 901 cannot generate a V_{boost+} voltage greater than the V_{dd} supply voltage, but less than the V_{dd} supply voltage plus the threshold voltage V_{tp} as required by the present invention.

Similarly, because charge pump control circuit 902 results in a V_{boost-} voltage less than or equal to the V_{SS} supply voltage minus the threshold voltage V_{tn}, this charge pump control circuit 902 cannot generate a V_{boost-} voltage less than the V_{SS} supply voltage, but greater than the V_{SS} supply voltage minus the absolute value of the threshold voltage V_{tn} as required by the present invention.

Fig. 10 is a schematic diagram of a V_{CCB} charge pump control circuit 1000 in accordance with the one embodiment of the present invention. V_{CCB} charge pump control circuit 1000 is used to replace charge pump control circuit 803 (Fig. 8), thereby creating a V_{CCB} reference voltage generation circuit that is capable of generating the desired V_{CCB} voltage. V_{CCB} charge pump control circuit 1000 includes p-channel transistors 1001-1003 and reference current sources 1004-1005. The source of p-channel transistor 1001 is coupled to receive the V_{dd} supply voltage, and the gate and drain of p-channel transistor 1001 are commonly connected to reference current source 1004. P-channel transistor 1001 is thereby connected as a diode between the V_{dd} voltage supply and reference current source 1004. Reference current source 1004 generates a reference current, I_{REFP}, which establishes a reference voltage, V_{REFP}, on the gate of p-channel transistor 1002.

P-channel transistor 1001 has a channel width of W_p. P-channel transistors 1001 and 1002 have the same channel lengths. However, p-channel transistor 1002 has a channel width of m times W_p, where m is a multiplying constant. The drain of transistor 1002 is connected to another reference current source 1005, which generates a reference current, I_{REFP1}. The source of transistor 1002 is connected to node V_P. Node V_p is also connected to the drain and gate of p-channel transistor 1003. The source of transistor 1003 is connected to receive the positive boosted voltage V_{CCB} from charge pump 802. If the reference currents I_{REFP} and I_{REFP1} are equal, and transistor

1002 has the same channel width as transistor 1001 (i.e., m=1), then node V_P will be held at a voltage equal to the V_{dd} supply voltage. Under these conditions, the positive boosted voltage V_{CCB} will be higher than the V_{dd} supply voltage by a voltage greater than the absolute value of the threshold voltage V_{tp} of p-channel transistor 1003.

In the present embodiment, reference current I_{REFP} is set approximately equal to reference current I_{REFP1}, and the multiplying constant m is set equal to four. Because the channel length of transistor 1002 is four times longer than the channel length of transistor 1001, the source-to-gate voltage of transistor 1002 is less than the source-to-gate voltage of transistor 1001. As a result, the voltage on node V_P is less than the V_{dd} supply voltage. For example, if reference currents I_{REFP} and I_{REFP1} are both set equal to about 50 μA, then the voltage on node V_P will be about 0.2 Volts less than the V_{dd} supply voltage. The channel width of transistor 1003 is selected to be relatively large (e.g., on the order of 50 μm) such that the source-to-gate voltage of transistor 1003 is approximately equal to the threshold voltage of transistor 1003 (e.g., 0.5 Volts). As a result, the V_{CCB} voltage is maintained at a voltage about 0.3 Volts greater than the V_{dd} supply voltage. The V_{CCB} voltage is therefore less than one threshold voltage greater than the V_{dd} supply voltage.

In another embodiment, p-channel transistor 1003 can be eliminated, such that the V_{CCB} voltage is provided directly to node V_P. However, in this embodiment, the channel width of transistor 1002 must be selected to smaller than the channel width W_p of transistor 1001. That is, the multiplier constant m must be selected to be less than one, such that the source-to-gate voltage of transistor 1002 is greater than the source-to-gate voltage of transistor 1001 by about 0.3 Volts (or another voltage that is less than the p-channel threshold voltage).

Fig. 11 is a schematic diagram of a V_{BBS} charge pump control circuit 1100 in accordance with the one embodiment of the present invention. V_{BBS} charge pump control circuit 1100 is used to replace charge pump control circuit 803 (Fig. 8), thereby creating a V_{BBS} reference voltage generation circuit that is capable of generating the desired V_{BBS} voltage. V_{BBS} charge pump control circuit 1100 includes n-channel transistors 1101-1102, p-channel transistor 1103 and reference current sources 1104-1105. The source of n-channel transistor 1101 is connected to receive the V_{SS} supply voltage. The drain and gate of transistor 1101 are commonly connected to reference current source 1104. Thus, transistor 1101 is connected as a diode. Reference current source 1104 is connected between the V_{dd} voltage supply and the commonly connected drain and gate drain of n-channel transistor 1101. Reference current source 1104 provides a reference current I_{REFN1} to n-channel transistor 1101. The reference current I_{REFN1} establishes a reference voltage, V_{REFN}, on the gate of n-channel transistor 1102.

N-channel transistor 1101 has a channel width of W_n. N-channel transistors 1101 and 1102 have the same channel lengths. However, n-channel transistor 1102 has a channel width of n times W_n, where n is a multiplying constant. The drain of transistor 1102 is connected to another reference current source 1105, which generates a reference current, I_{REFN}. The source of transistor 1102 is connected to node V_N. Node V_N is also connected to the source of p-channel transistor 1103. The drain and gate of transistor 1103 are commonly connected to receive the negative boosted voltage V_{BBS}. If the reference currents I_{REFN} and I_{REFN1} are equal, and transistor 1102 has the same channel width as transistor 1101 (i.e., n=1), then node V_N will be held at a voltage equal to the V_{SS} supply voltage. Under these conditions, the negative boosted voltage V_{BBS} will be

regulated at a voltage approximately one threshold voltage (V_{tp}) below the V_{SS} supply voltage.

In the present embodiment, reference current I_{REFN} is set approximately equal to reference current I_{REFN1}, and the multiplying constant n is set equal to four. Because the channel width of transistor 1102 is four times longer than the channel width of transistor 1101, the source-to-gate voltage of transistor 1102 is less than the source-to-gate voltage of transistor 1101. As a result, the voltage potential on node V_N is higher than the V_{SS} supply voltage. For example, if reference currents I_{REFN} and I_{REFN1} are both set equal to about 50 μA, then the voltage on node V_N will be about 0.2 Volts greater than the V_{SS} supply voltage. The channel width of transistor 1103 is selected to be relatively large (e.g., on the order of 50 μm) such that the source-to-gate voltage of transistor 1103 is approximately equal to the threshold voltage of transistor 1103 (e.g., 0.5 Volts). As a result, the V_{BBS} voltage is maintained at a voltage about 0.3 Volts less than the V_{SS} supply voltage. The V_{BBS} voltage is therefore less than one threshold voltage than the V_{SS} supply voltage.

In another embodiment, p-channel transistor 1103 can be eliminated, such that the V_{BBS} voltage is provided directly to node V_N. However, in this embodiment, the channel width of transistor 1102 must be selected to smaller than the channel width W_n of transistor 1101. That is, the multiplier constant n must be selected to be less than one, such that the source-to-gate voltage of transistor 1102 is greater than the source-to-gate voltage of transistor 1101 by about 0.3 Volts (or another voltage that is less than the p-channel threshold voltage).

It is desirable to keep the V_{CCB} and V_{BBS} voltages relatively constant for variations in temperature. In general, the transistor threshold voltage V_t tends to decrease as the temperature increases. To compensate for this temperature effect, reference current sources 1004

and 1104 are constructed such that reference currents I_{REFP} and I_{REFN1} have negative temperature coefficients (i.e., reference currents I_{REFP} and I_{REFN1} decrease as the temperature increases).

Fig. 12 is a schematic diagram of reference current source 1004 in accordance with one embodiment of the present invention. Reference current source 1004 includes p-channel transistors 1201-1202, resistor 1203 and n-channel transistors 1204-1206. Resistor 1203 is connected between the V_{dd} voltage supply and the gate of transistor 1201, thereby setting the bias for transistor 1201. The current I_R through resistor 1203 is equal to the threshold voltage V_{tp} of transistor 1201 divided by the resistance of resistor 1203. The current I_R is therefore directly related to the threshold voltage V_{tp}. The current I_R flows through p-channel transistor 1202 and n-channel transistor 1205.

The gate and source of transistor 1202 are coupled to the drain and gate, respectively, of transistor 1201. The voltage on the gate of transistor 1202 is translated to the drain of transistor 1202. N-channel transistors 1204-1206 each have a source terminal coupled to the V_{SS} voltage supply and a gate terminal coupled to the drain of transistor 1202, thereby forming a current mirror circuit. The current I_R is thereby translated to transistor 1206. As a result, the current through n-channel transistor 1206 (i.e., I_{REFP}) is directly related to the threshold voltage V_{tp} of p-channel transistor 1201.

Reference current source 1004 provides temperature compensation as follows.

As the temperature increases, the threshold voltages V_{tp} of transistors 1002 and 1003 (Fig. 10) decrease, thereby causing the V_{CCB} voltage to decrease. However, as the temperature increases, the threshold voltage V_{tp} of transistor 1201 (Fig. 12) decreases. In response, the current I_R decreases, thereby reducing the I_{REFP} current.

As a result, the gate-to-source voltage of p-channel transistor 1001 (Fig. 10) decreases, thereby increasing the V_{REFP} voltage. The increased V_{REFP} voltage, in turn, causes the voltage V_P to increase, thereby increasing the V_{CCB} voltage. The temperature effect of the threshold voltage V_{tp} of transistors 1002 and 1003 is thereby partially compensated by the negative temperature coefficient of the I_{REFP} current. In this manner, reference current source 1004 provides temperature compensation to V_{CCB} pump control circuit 1000.

Fig. 13 is a schematic diagram of reference current source 1104 in accordance with one embodiment of the present invention. Because reference current source 1104 is similar to reference current source 1004 (Fig. 12), similar elements in Figs. 12 and 13 are labeled with similar reference numbers. Thus, reference current source 1104 includes p-channel transistors 1201-1202, resistor 1203 and n-channel transistors 1204-1205. In addition, reference current source 1104 includes a p-channel transistor 1301 having a gate coupled to the gate of transistor 1201, and a source coupled to receive the V_{dd} supply voltage.

Reference current source 1104 provides temperature compensation as follows.

As the temperature increases, the threshold voltages V_t of transistors 1102 and 1103 (Fig. 11) decrease, thereby causing the V_{BBS} voltage to increase. However, as the temperature increases, the threshold voltage V_{tp} of p-channel transistor 1201 decreases. As a result, the current I_R decreases. Because transistors 1201 and 1301 are coupled to form a current mirror circuit, the decrease in the current I_R results in a decrease in the current I_{REFN1}. A decrease in the current I_{REFN1}, in turn, causes a decrease in the voltage V_{REFN} (Fig. 11). The decrease in V_{REFN} results in a decrease of the voltage V_N, which in turn, causes a decrease in the V_{BBS} voltage. In this

manner, reference current source 1104 provides temperature compensation to V_{BBS} pump control circuit 1100.

If the I_{REFP1} current is temperature independent, then reference current source 1004 (Fig. 12) mainly compensates for the temperature effect of transistor 1002, thereby leaving the temperature effect of transistor 1003 largely uncompensated. Similarly, if the I_{REFN} current is temperature independent, then reference current source 1104 (Fig. 13) mainly compensates for the temperature effect of transistor 1102, leaving the temperature effect of transistor 1103 largely uncompensated. To compensate for the uncompensated temperature effects of transistors 1003 and 1103, reference current sources 1005 and 1105 are constructed such that reference currents I_{REFP1} and I_{REFN} have positive temperature coefficients (i.e., reference currents I_{REFP1} and I_{REFN} increase as the temperature increases).

Fig. 14 is a schematic diagram of reference current source 1005 in accordance with one embodiment of the present invention. Reference current source 1005 includes p-channel transistors 1401-1403, n-channel transistors 1411-1414, PNP bipolar transistors 1421-1422 and resistor 1431. Transistors 1401, 1411 and 1421 are connected in series between the V_{dd} and V_{ss} voltage supplies. Transistors 1402, 1412 and 1422 and resistor 1431 are connected in series between the V_{dd} and V_{ss} voltage supplies. Transistor 1403 is connected in series with parallel-connected transistors 1413-1414 between the V_{dd} and V_{ss} voltage supplies. P-channel transistors 1401-1403 are configured to form a current mirror circuit, such that the same current flows through all three of these transistors 1401-1403. The emitter of transistor 1422 is selected to be m times larger than the emitter of transistor 1421, where m is a multiplying constant. In the described embodiment, the multiplying constant m is equal to 4. The multiplying constant m and the resistor

value of resistor 1431 is selected such that the resultant current I_{REFP1} is approximately equal to I_{REFP}. The voltages at the sources of transistors 1411 and 1412 are maintained at the same voltage by transistors 1401-1402 and 1411-1412. As a result, the voltage across transistor 1421 is equal to the voltage across resistor 1431 and transistor 1422.

The operation of reference current source 1005 is well documented in references such as "Analysis and Design of Analog Integrated Circuits", by P.R. Gray and R.G. Meyer, pp. 330-333, which is hereby incorporated by reference. The current I_R through resistor 1431 is equal to $V_T/R \ln(m)$. $V_T = kT/q$, where k is equal to Boltzmann's constant, T is equal to absolute temperature, and q is equal to electron charge. The current through resistor 1431 is therefore directly related to temperature. The current I_R through resistor 1431 is translated to create the I_{REFP1} current through transistors 1403 and 1413-1414. As a result, the I_{REFP1} current is directly related to temperature. Thus, as temperature increases, the I_{REFP1} current increases. The increased I_{REFP1} current increases the gate-to-source voltages of transistors 1002 and 1003 in Fig. 10, thereby offsetting the decrease in the threshold voltage V_{tp} of transistor 1003 which occurs with increases in temperature. As described above, the decrease of the threshold voltage V_{tp} of transistor 1003 tends to decrease the V_{CCB} voltage. However, the increased I_{REFP1} current tends to increase the V_{CCB} voltage. The net result is that the V_{CCB} voltage is maintained relatively constant throughout the operating temperature range.

Fig. 15 is a schematic diagram of reference current source 1105 in accordance with one embodiment of the present invention. Reference current source 1105 includes p-channel transistors 1401-1402 and 1501, n-channel transistors 1411-1412, PNP bipolar transistors 1421-1422 and resistor 1431. Transistors 1401-1402, 1411-1412,

1421-1422 and resistor 1432 are connected in the manner described above for Fig. 14. In addition, the gate of transistor 1501 is commonly connected to the gates of transistors 1401-1402. As described above, the current I_R through resistor 1431 is directly related to temperature. Thus, as the temperature increases, the I_R current through resistor 1431 increases. This increased current is translated to transistor 1501, thereby resulting in an increased I_{REFN} current. The increased I_{REFN} current increases the gate-to-source voltages of transistors 1102 and 1103 in Fig. 11, thereby offsetting the decrease in threshold voltage V_{tp} of transistor 1103 in Fig. 11. As described above, the decrease in the threshold voltage V_{tp} of transistor 1103 tends to increase the V_{BBS} voltage. However, the increased I_{REFN} current tends to decrease the V_{BBS} voltage. The result is that the V_{BBS} voltage is maintained relatively constant in the operating temperature range of the reference current circuit 1104.

Fig. 16 is a schematic diagram illustrating reference current circuit 1600 in accordance with another embodiment of the present invention. Reference current circuit 1600 combines reference current circuits 1004 and 1104 in a single circuit, thereby reducing the required layout area of the resulting circuit. Similar elements in Figs. 12, 13 and 16 are labeled with similar reference numbers. Reference current circuit 1600 operates in the same manner as reference current circuits 1104 and 1104.

Fig. 17 is a schematic diagram illustrating reference current circuit 1700 in accordance with another embodiment of the present invention. Reference current circuit 1700 combines reference current circuits 1005 and 1105 in a single circuit, thereby reducing the required layout area of the resulting circuit. Similar elements in Figs. 14, 15 and 17 are labeled with similar reference numbers. Reference current circuit 1700 operates in the manner as reference current circuits 1005 and 1105.

The preferred embodiment described above uses PMOS transistors for the memory cells. The p-channel transistors are fabricated in N-well on P-substrate. In another embodiment, the memory cells can be fabricated using NMOS transistors. In such an embodiment, the word line is activated high and deactivated low.

Fig. 18 is a schematic diagram illustrating word line driver circuit 1600 and a V_{BBC} coupling circuit 1800 that can be used to drive memory cells constructed from NMOS transistors. Word line driver circuit 1600 includes p-channel pull-up transistor 401 and n-channel pull-down transistor 403, which were described above in connection with word line driver 400 (Fig. 4). The remainder of word line driver 1600 is a reciprocal circuit of word line driver 400. The reciprocal circuit is obtained by replacing PMOS transistors NMOS transistors, replacing NMOS transistors with PMOS transistors, replacing connections to the V_{dd} voltage supply with connections to the V_{SS} voltage supply, and replacing connections to the V_{SS} voltage supply with connections to the V_{dd} voltage supply. Thus, in addition to pull up and pull down transistors 401 and 403, word line driver 1600 includes n-channel transistor 1601, p-channel transistors 1602-1603 and row address decoder 1610.

N-channel pull-down transistor 403 of word line driver 400 is coupled directly to V_{BBS} voltage generator 800. In this embodiment, the V_{BBS} voltage generator provides a V_{BBS} voltage about -0.3 V below the V_{SS} supply voltage. The p-channel pull-up transistor 401 of word line driver 400 is coupled to receive a V_{BBC} voltage from V_{BBC} coupling circuit 1800. Row address decoder 1610 provides control signals X_i# and X_j, which are the inverse of the control signals X_i and X_j# provided by row address decoder 410 (Fig. 4).

V_{BBC} coupling circuit 1800 is the reciprocal the coupling circuit 600 of Fig. 6. Thus, V_{BBC} coupling

circuit 1800 includes n-channel transistors 1801-1803, p-channel transistor 1804 and inverters 1811-1814, as illustrated.

Prior to activating word line 303, the X_i# signal is high and the X_j signal is low. Under these conditions, transistor 1602 is turned on, thereby applying the Vdd supply voltage to the gates of transistors 401 and 403. As a result, pull-down transistor 403 turns on, thereby providing the VBBS voltage to word line 303. Also under these conditions, the chain of inverters 1811-1814 provides a logic low signal to node N1, thereby turning on p-channel transistor 1804. As a result, the V_{BBC} supply line is maintained at the V_{dd} supply voltage. Also, prior to activating word line 303, the sub-threshold leakage of transistor 1802 pulls node N2 to a voltage greater than one threshold voltage drop (V_t) below V_{CCB}, thereby preventing transistor 1801 from turning on.

The X_i# signal is driven low and then the X_j signal is driven high to activate word line 303. Under these conditions, pull up transistor 401 turns on, thereby coupling word line 303 to the V_{BBC} voltage coupling circuit 1800. Immediately after transistor 401 is turned on, the high state of the X_j signal is propagating through the chain of inverters 1811-1814 and has not reached node N1. During this time, p-channel transistor 1804 remains on, coupling the V_{BBC} supply line to receive the V_{dd} supply voltage. Also during this time, the low state of node N1 pulls the source and drain of capacitor-coupled transistor 1803 to a low state. Transistor 1802 is connected as an MOS diode with its gate and drain connected to the V_{CCB} supply line. Transistor 1802 therefore limits the voltage at node N2 to no more than one threshold voltage (V_t) below the V_{CCB} voltage, or to a potential approximately equal to the V_{dd} supply voltage. Consequently, capacitor 1803 is initially charged to a voltage approximately equal to the

V_{dd} supply voltage (i.e., the voltage across transistor 1803 is approximately equal to V_{dd}).

When the high state of the X_j signal reaches node N1, transistor 1804 is turned off, thereby de-coupling the V_{BBC} voltage supply line from the V_{dd} voltage supply terminal. The high voltage at node N1 also causes capacitor 1803 to pull node N2 up to a voltage equal to $2V_{dd}$. The $2V_{dd}$ voltage at node N2 turns on n-channel transistor 1801, thereby coupling the V_{CCB} voltage supply line to the V_{BBC} voltage supply line.

Although the invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications which would be apparent to a person skilled in the art. Thus, the invention is limited only by the following claims.

CLAIMS

What is claimed is:

1. A memory system that operates in response to a positive supply voltage and a ground supply voltage, the memory system comprising:

a dynamic random access memory (DRAM) cell;

a word line coupled to the DRAM cell, wherein the word line is activated to access the DRAM cell;

a word line driver coupled to the word line; and

a positive boosted voltage generator for providing a positive boosted voltage greater than the positive supply voltage and less than one transistor threshold voltage greater than the positive supply voltage, the positive boosted voltage generator being coupled to the word line driver.

2. The memory system of Claim 1, wherein the word line driver comprises a p-channel transistor coupled between the word line and the positive boosted voltage generator, and an n-channel transistor coupled to the word line.

3. The memory system of Claim 2, further comprising a negative boosted voltage generator for providing a negative boosted voltage less than the ground supply voltage, the negative boosted voltage generator being coupled to the word line driver.

4. The memory system of Claim 3, wherein the negative boosted voltage is less than the ground supply voltage by a voltage less than the absolute value of one transistor threshold voltage.

5. The memory system of Claim 4, wherein the DRAM cell comprises:

a first p-channel transistor having a gate coupled to the word line; and

a second p-channel device coupled to the first p-channel transistor, the second p-channel device being configured as a storage capacitor.

6. The memory system of Claim 1, wherein the memory system is fabricated using a conventional logic process.

7. The memory system of Claim 3, further comprising a coupling circuit coupled between the word line driver and the negative boosted voltage generator, the coupling circuit being configured to provide the ground supply voltage to the word line driver when the word line is first activated, the coupling circuit further being configured to provide the negative boosted voltage to the word line driver when the voltage on the word line falls below the positive supply voltage.

8. The memory system of Claim 7, wherein the coupling circuit comprises:

a first transistor coupled between the word line driver and a terminal providing the ground supply voltage;

a second transistor coupled between the word line driver and the negative boosted voltage generator; and

a delay chain coupled to a gate of the first transistor.

9. The memory system of Claim 8, further comprising:

a capacitor coupled between the delay chain and a gate of the second transistor; and

a diode element coupled between the gate of the second transistor and the negative boosted voltage generator.

10. The memory system of Claim 3, further comprising a coupling circuit coupled between the n-channel transistor and the negative boosted voltage generator, the coupling circuit being configured to couple the negative boosted voltage generator to the n-channel transistor when the word line is activated, and the coupling circuit being configured to provide the ground supply voltage to the n-channel transistor when the word line is not activated.

11. A memory system that operates in response to a positive supply voltage and a ground supply voltage, the memory system comprising:

a dynamic random access memory (DRAM) cell;

a word line coupled to the DRAM cell, wherein the word line is activated to access the DRAM cell;

a word line driver coupled to the word line; and

a negative boosted voltage generator for providing a negative boosted voltage less than the ground supply voltage by a voltage less than the absolute value of one transistor threshold voltage, wherein the negative boosted voltage generator is coupled to the word line driver.

12. The memory system of Claim 11, wherein the word line driver comprises an n-channel transistor coupled between the word line and the negative boosted voltage generator, and a p-channel transistor coupled to the word line.

13. The memory system of Claim 12, further comprising a positive boosted voltage generator for providing a positive boosted voltage greater than the

positive supply voltage, the positive boosted voltage generator being coupled to the word line driver.

14. The memory system of Claim 13, wherein the positive boosted voltage is greater than the positive supply voltage by less than one transistor threshold voltage.

15. The memory system of Claim 13, further comprising a coupling circuit between the p-channel transistor and the positive boosted voltage generator, the coupling circuit being configured to couple the positive boosted voltage generator to the p-channel transistor when the word line is activated, and the coupling circuit being configured to provide the positive supply voltage to the p-channel transistor when the word line is not activated.

16. The memory system of Claim 15, wherein the DRAM cell comprises:

a first n-channel transistor having a gate coupled to the word line; and

a second n-channel device coupled to the first n-channel transistor, the second n-channel device being configured as a storage capacitor.

17. The memory system of Claim 11, wherein the memory system is fabricated using a conventional logic process.

18. The memory system of Claim 13, further comprising a coupling circuit coupled between the word line driver and the positive boosted voltage generator, the coupling circuit being configured to provide the positive supply voltage to the word line driver when the word line is first activated, the coupling circuit further being configured to provide the positive boosted voltage

to the word line driver when the voltage on the word line rises above the ground supply voltage.

19. The memory system of Claim 18, wherein the coupling circuit comprises:

a first transistor coupled between the word line driver and a terminal providing the positive supply voltage;

a second transistor coupled between the word line driver and the positive boosted voltage generator; and

a delay chain coupled to a gate of the first transistor.

20. The memory system of Claim 19, further comprising:

a capacitor coupled between the delay chain and a gate of the second transistor; and

a diode element coupled between the gate of the second transistor and the positive boosted voltage generator.

21. A method of driving a word line coupled to a dynamic random access memory (DRAM) cell, the method comprising the steps of:

generating a negative boosted voltage less than a ground supply voltage by less than one transistor threshold voltage;

providing the ground supply voltage to the word line when the word line is first activated; and then

providing the negative boosted voltage to the word line when the voltage on the word line falls below a positive supply voltage.

22. The method of Claim 21, further comprising the steps of:

generating a positive boosted voltage greater than a positive supply voltage by less than one transistor threshold voltage; and

driving the word line with the positive boosted voltage when the DRAM cell is not being accessed.

23. A method of driving a word line coupled to a dynamic random access memory (DRAM) cell, the method comprising the steps of:

generating a positive boosted voltage greater than a positive supply voltage by less than one transistor threshold voltage;

providing the positive supply voltage to the word line when the word line is first activated; and then

providing the positive boosted voltage to the word line when the voltage on the word line rises above a ground supply voltage.

24. The method of Claim 23, further comprising the steps of:

generating a negative boosted voltage less than a ground supply voltage by less than one transistor threshold voltage; and

driving the word line with the negative boosted voltage when the DRAM cell is not being accessed.

25. A charge pump control circuit for generating a positive boosted voltage that is greater than a positive supply voltage by less than one threshold voltage, the charge pump control circuit comprising:

a first p-channel transistor having a source coupled to the positive supply voltage, the first p-channel transistor having a first channel width;

a first reference current source coupled to a drain of the first p-channel transistor;

a second p-channel transistor having a gate coupled to a gate of the first p-channel transistor, the second p-channel transistor having a second channel width, wherein the second channel width is greater than the first channel width;

a second reference current source coupled to a drain of the second p-channel transistor; and

a third p-channel transistor having a gate and a drain connected to a source of the second p-channel transistor, the third p-channel transistor further having a source coupled to receive the positive boosted voltage.

26. The charge pump control circuit of Claim 25, wherein the first reference current source has a negative temperature coefficient.

27. The charge pump control circuit of Claim 25, wherein the second reference current source has a positive temperature coefficient.

28. A charge pump control circuit for generating a negative boosted voltage that is less than a ground supply voltage by less than one threshold voltage, the charge pump control circuit comprising:

a first n-channel transistor having a source coupled to the ground supply voltage, the first p-channel transistor having a first channel width;

a first reference current source coupled to a drain of the first n-channel transistor;

a second n-channel transistor having a gate coupled to a gate of the first n-channel transistor, the second n-channel transistor having a second channel width, wherein the second channel width is greater than the first channel width;

a second reference current source coupled to a drain of the second n-channel transistor; and

a p-channel transistor having a source connected to a source of the second n-channel transistor, the p-channel transistor further having gate and a drain coupled to receive the negative boosted voltage.

29. The charge pump control circuit of Claim 28, wherein the first reference current source has a negative temperature coefficient.

30. The charge pump control circuit of Claim 29, wherein the second reference current source has a positive temperature coefficient.

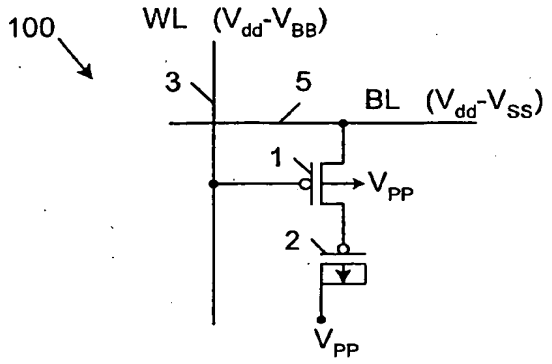


FIG. 1A
(PRIOR ART)

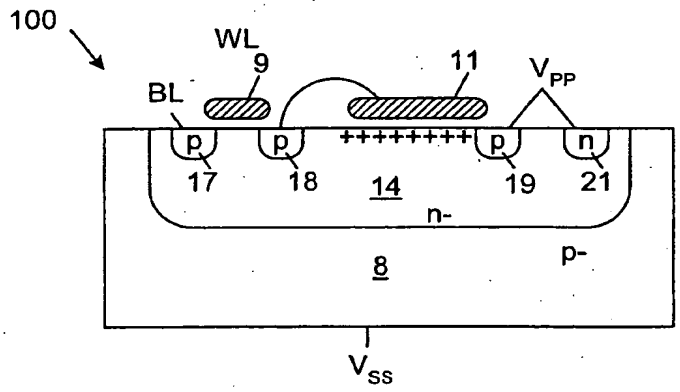


FIG. 1B
(PRIOR ART)

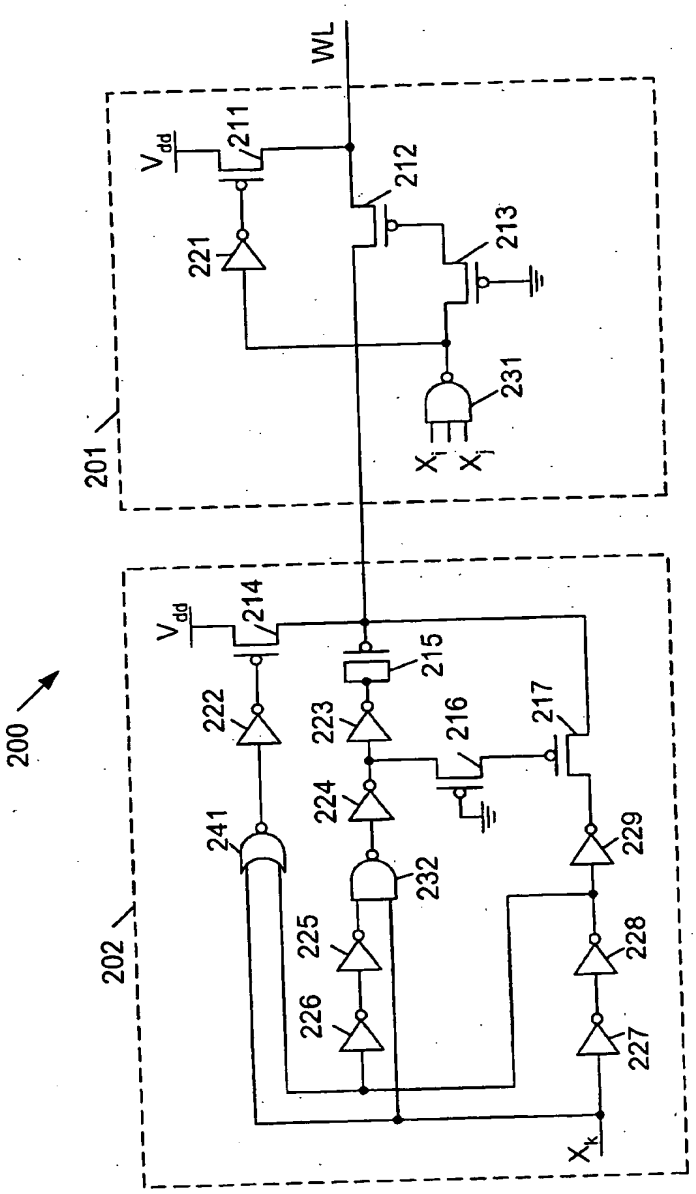


FIG. 2
(PRIOR ART)

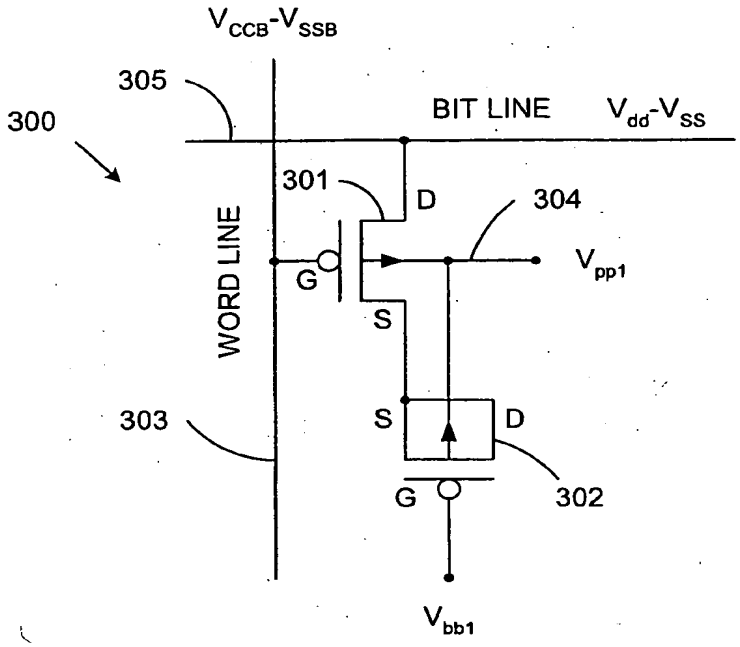

V_{CCB}-V_{SSB}
305
300
BIT LINE
V_{dd}-V_{SS}
301
D
304
V_{pp1}
G
S
WORD LINE
303
S
D
G
302
V_{bb1}

FIG. 3A

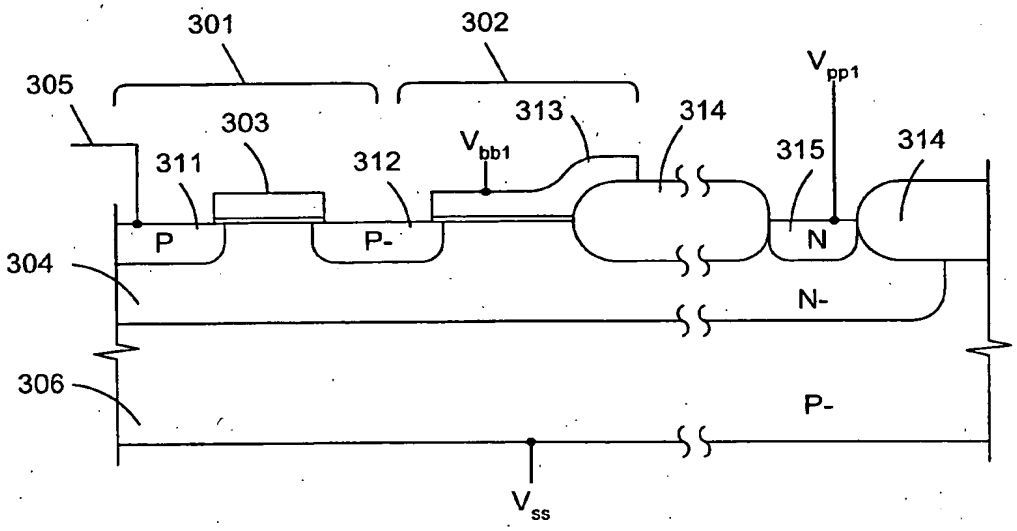

301
302
305
303
313
314
V_{pp1}
311
312
V_{bb1}
315
314
P
P-
N
304
N-
306
P-
V_{ss}

FIG. 3B

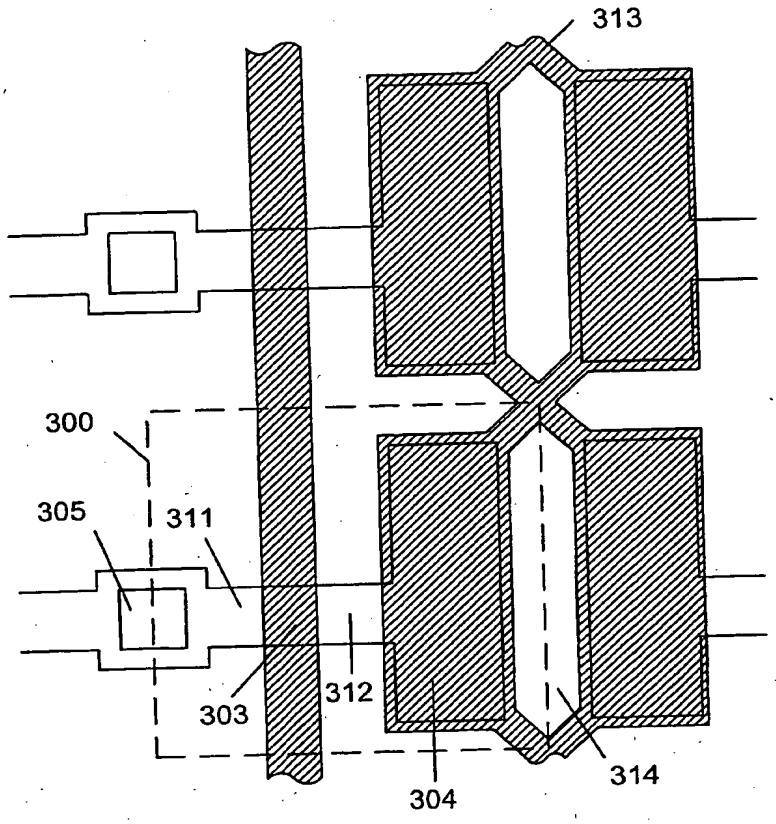

313
300
305
311
303
312
304
314

FIG. 3C

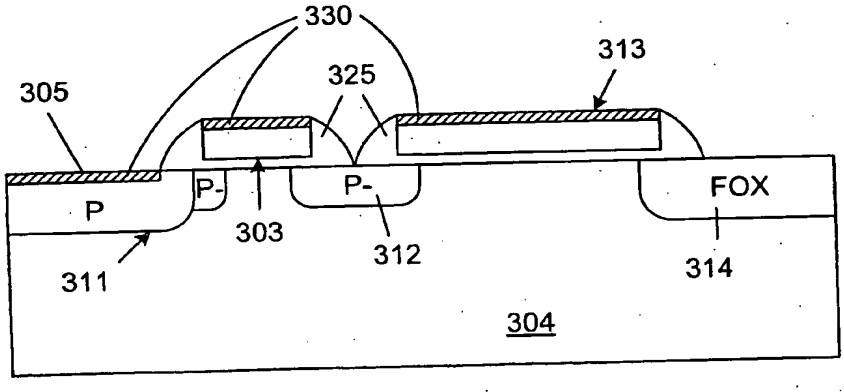

330
313
325
305
P-
P-
P
FOX
303
312
311
314
304

FIG. 3D

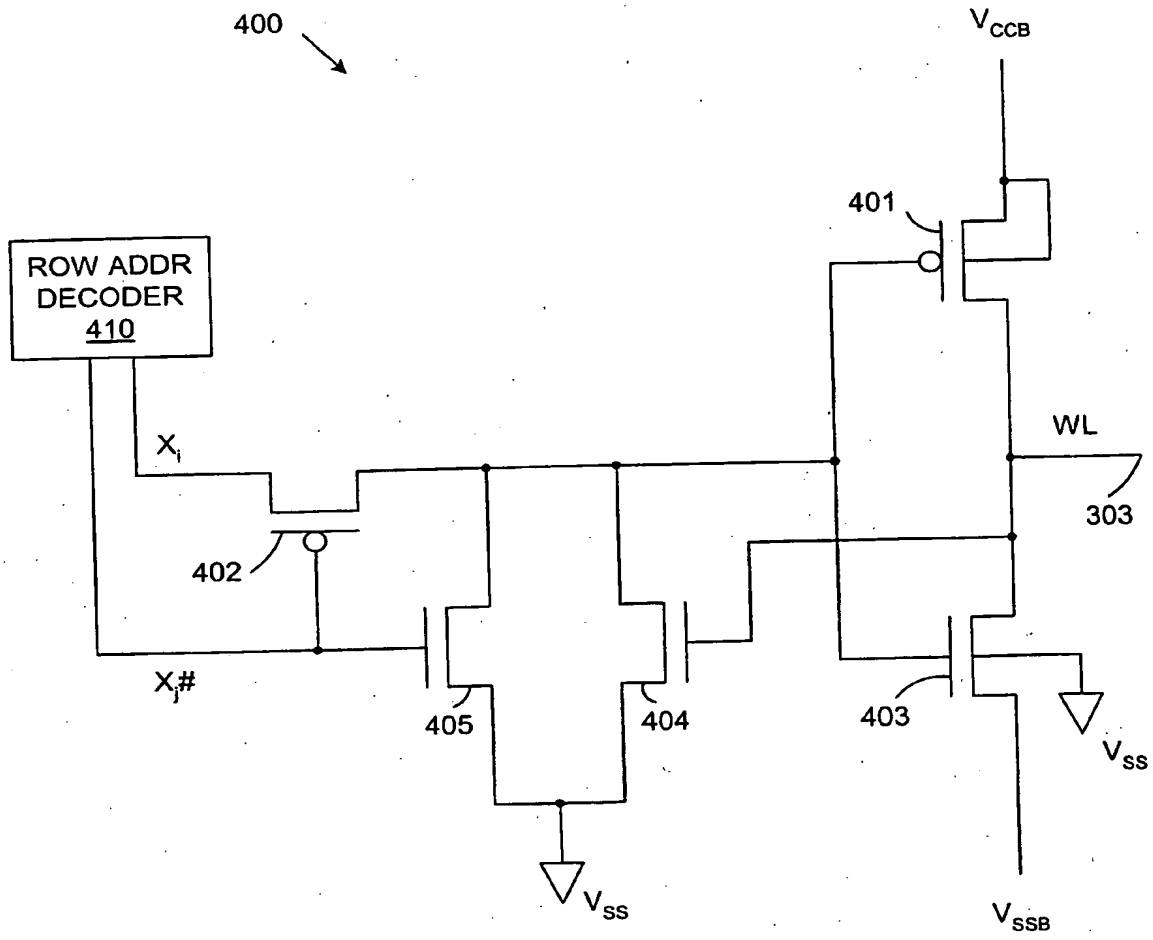

400
V_{CCB}
401
ROW ADDR
DECODER
410
X_i
WL
303
402
X_j#
405
404
403
V_{SS}
V_{SS}
V_{SSB}

FIG. 4

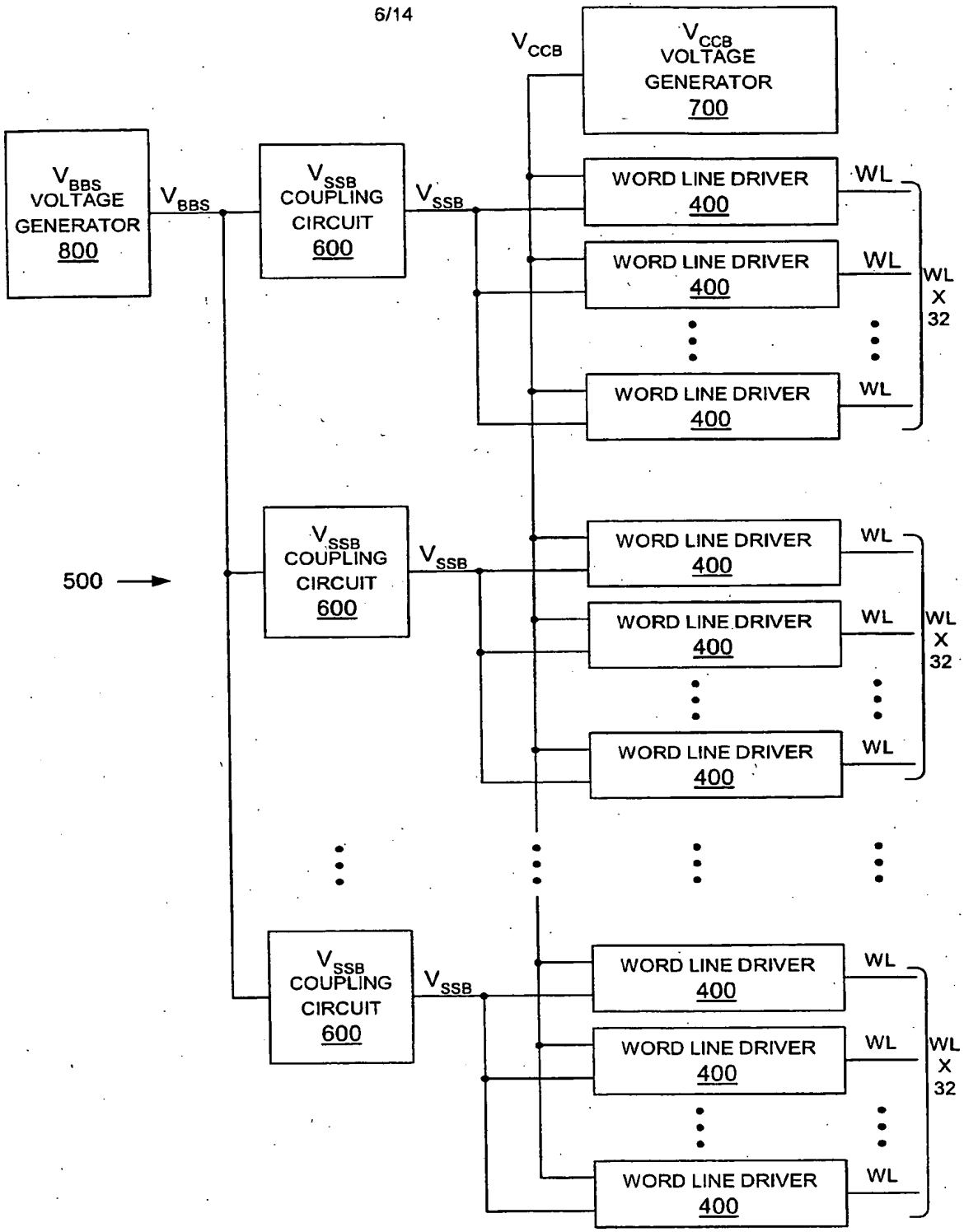

V_{CCB}
V_{CCB} VOLTAGE GENERATOR 700
V_{BBS} VOLTAGE GENERATOR 800
V_{BBS}
V_{SSB} COUPLING CIRCUIT 600
V_{SSB}
WORD LINE DRIVER 400
WL
WL X 32
500

FIG. 5

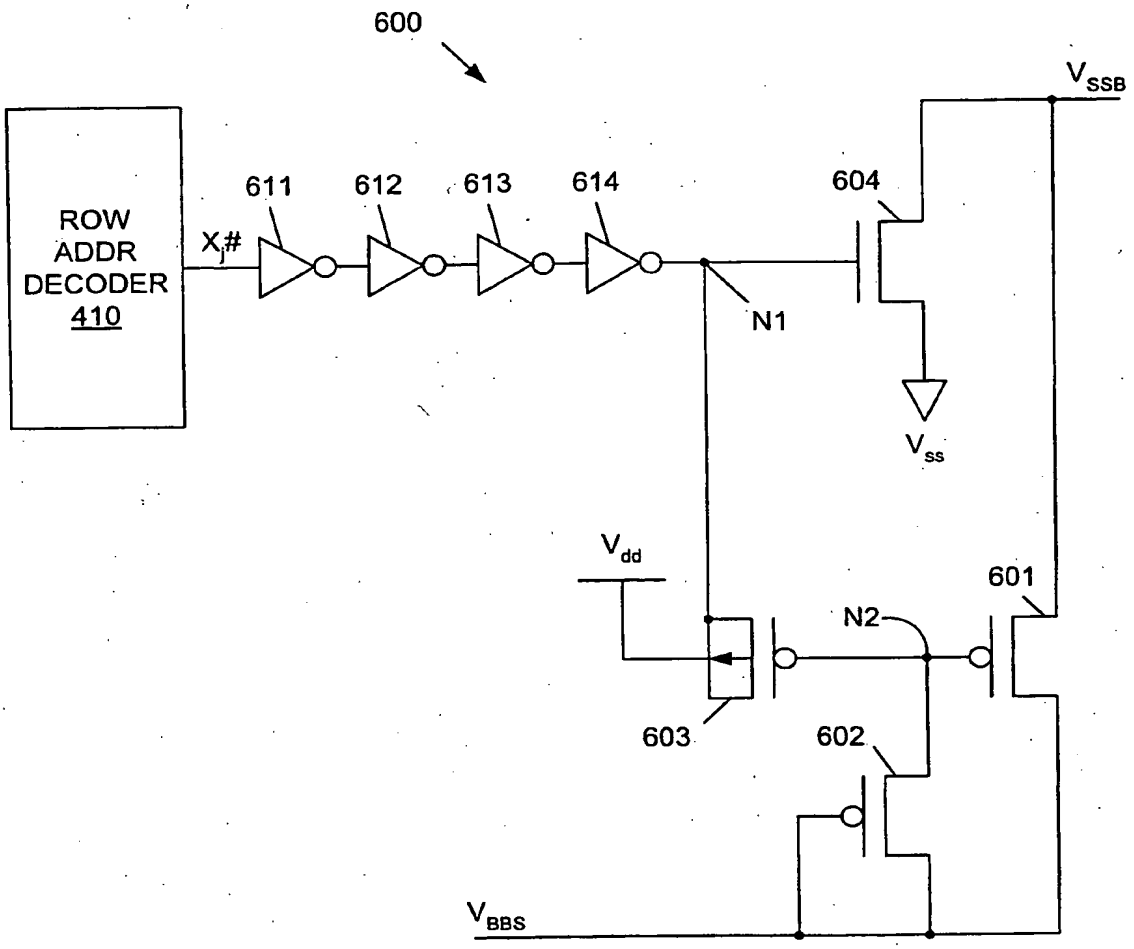

600
ROW
ADDR
DECODER
410
X_j#
611
612
613
614
604
N1
V_SSB
V_ss
V_dd
601
N2
603
602
V_BBS

FIG. 6

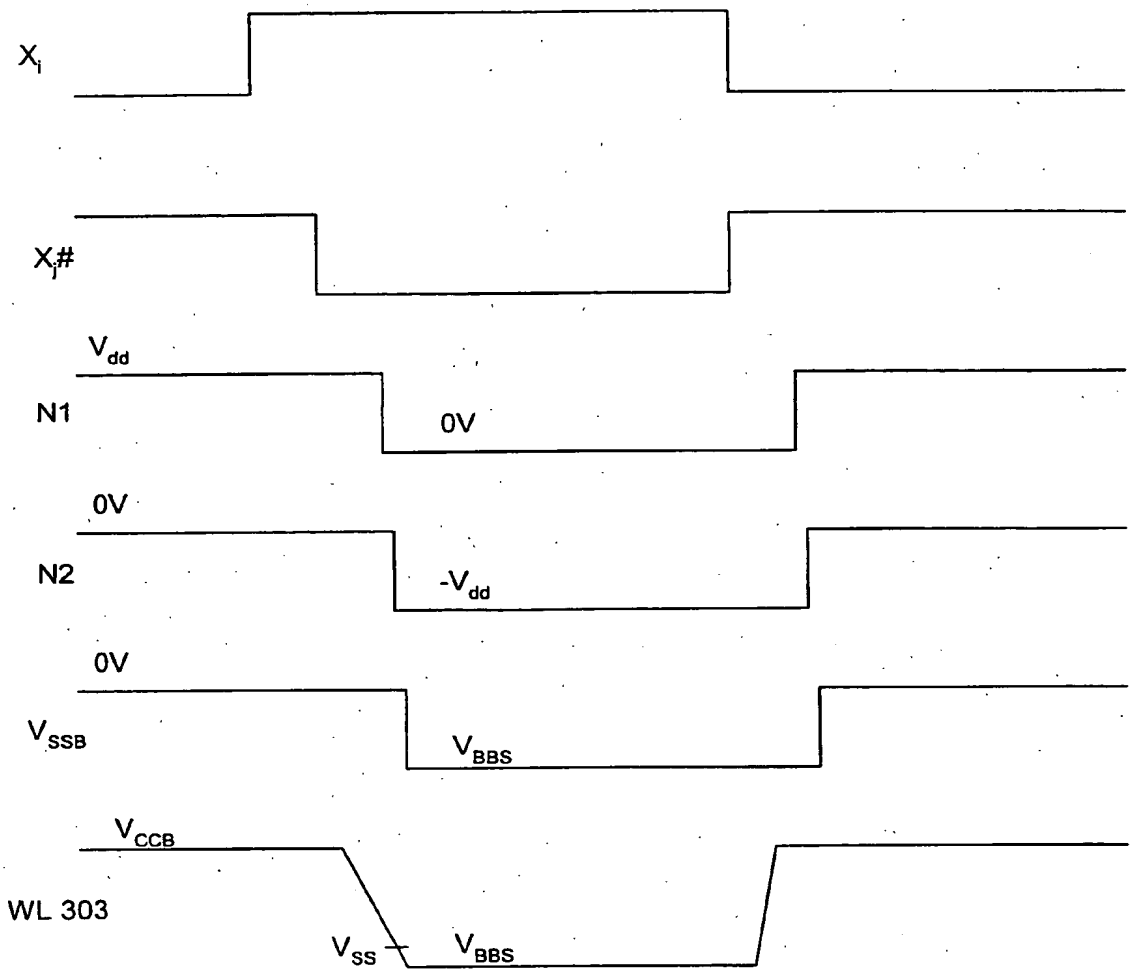


FIG. 7

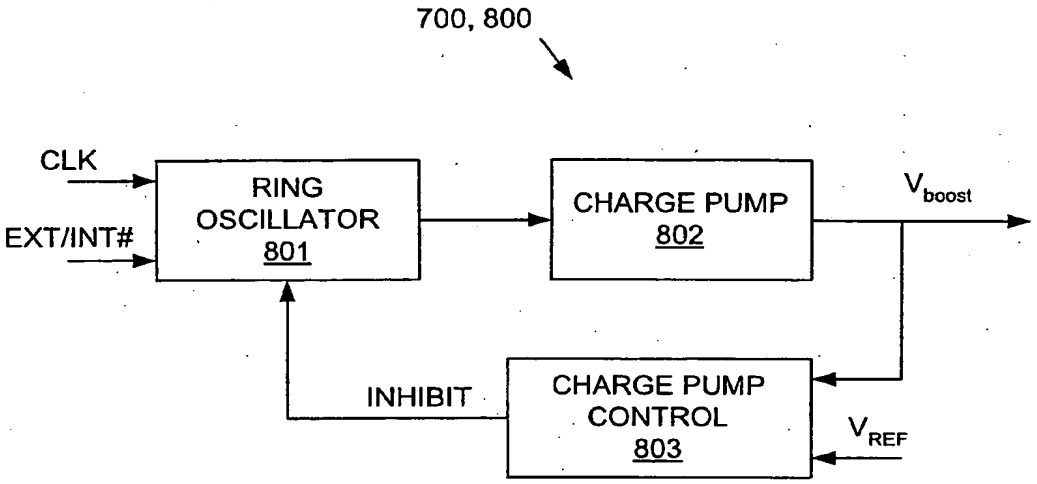


FIG. 8
(PRIOR ART)

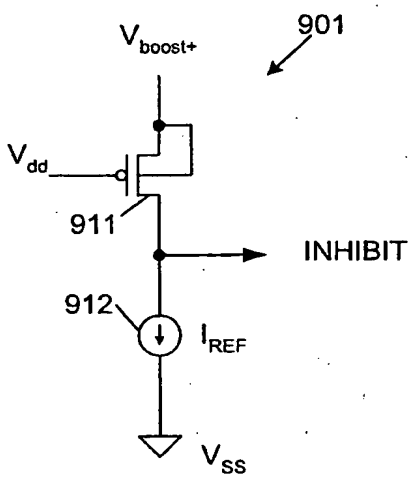


FIG. 9A
(PRIOR ART)

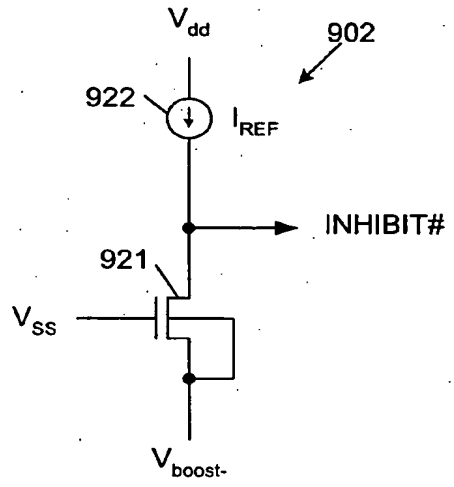


FIG. 9B
(PRIOR ART)

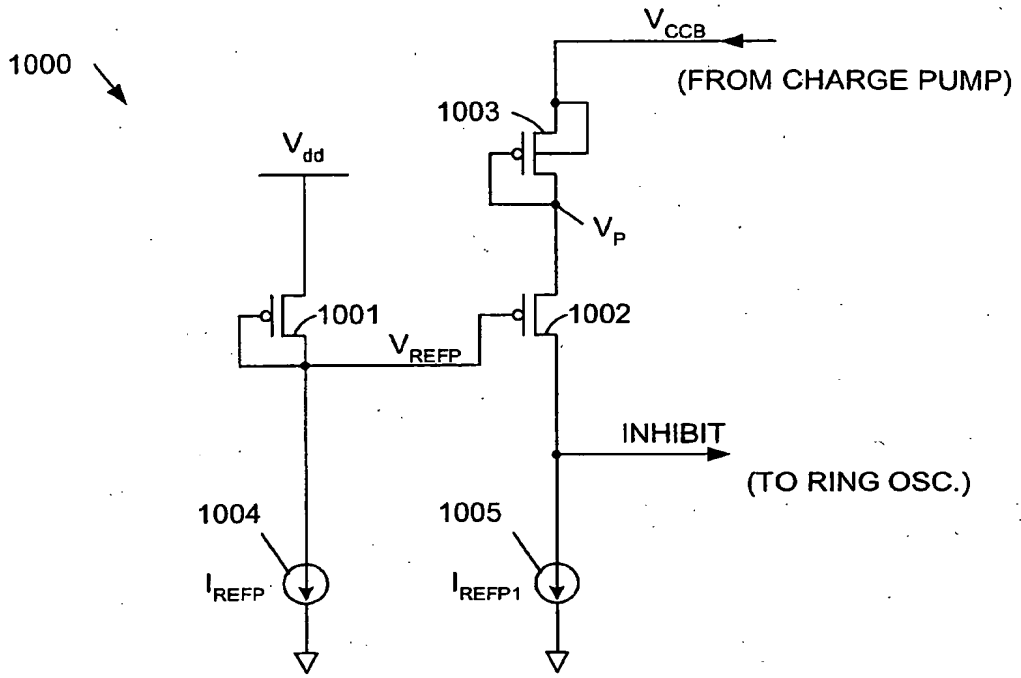

1000
V_{CCB}
(FROM CHARGE PUMP)
1003
V_{dd}
V_P
1001
1002
V_{REFP}
INHIBIT
(TO RING OSC.)
1004
1005
I_{REFP}
I_{REFP1}

FIG. 10

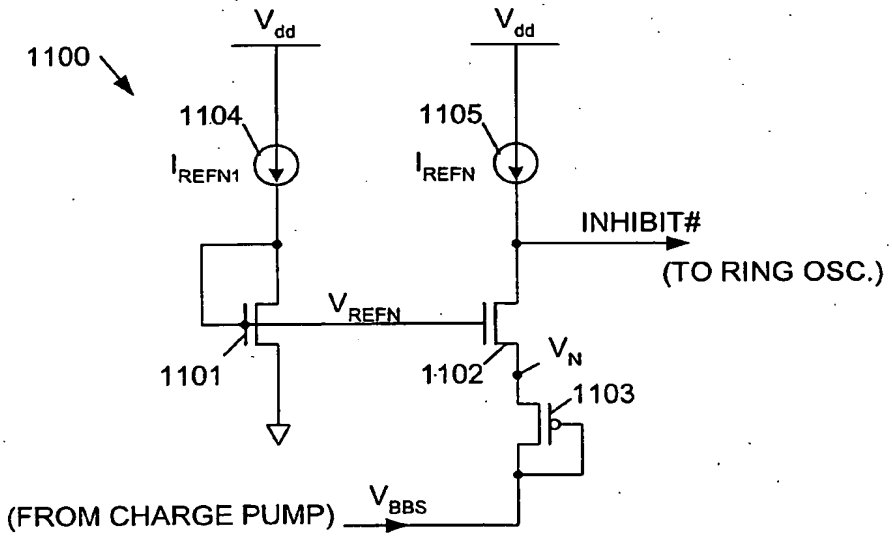

1100
V_{dd}
V_{dd}
1104
1105
I_{REFN1}
I_{REFN}
INHIBIT#
(TO RING OSC.)
V_{REFN}
V_N
1101
1102
1103
(FROM CHARGE PUMP)
V_{BBS}

FIG. 11

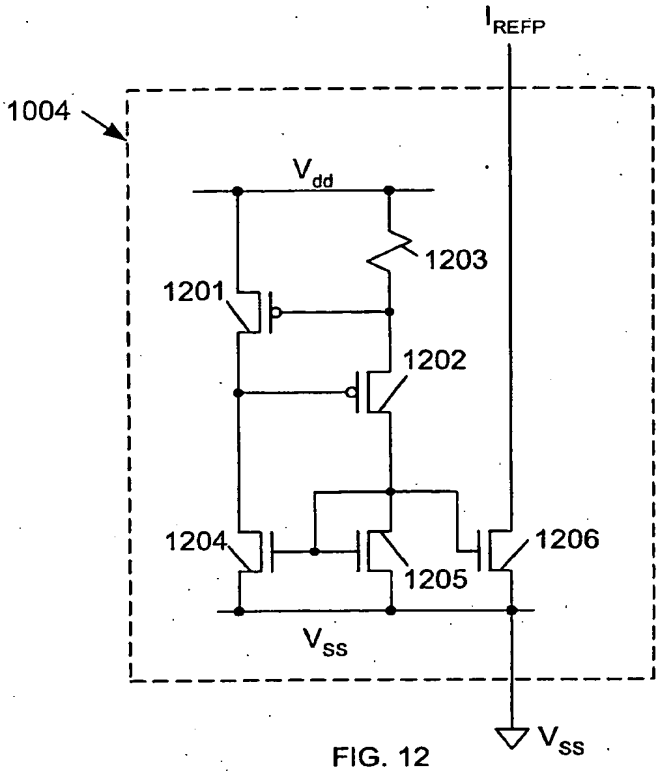

I_{REFP}
1004
V_{dd}
1203
1201
1202
1204
1205
1206
V_{SS}
V_{SS}

FIG. 12

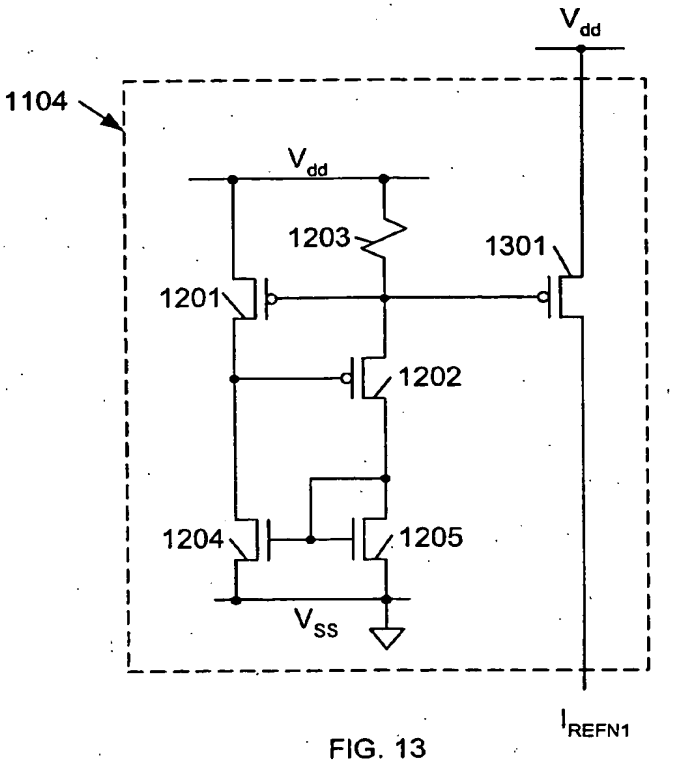

V_{dd}
1104
V_{dd}
1203
1301
1201
1202
1204
1205
V_{SS}
I_{REFN1}

FIG. 13

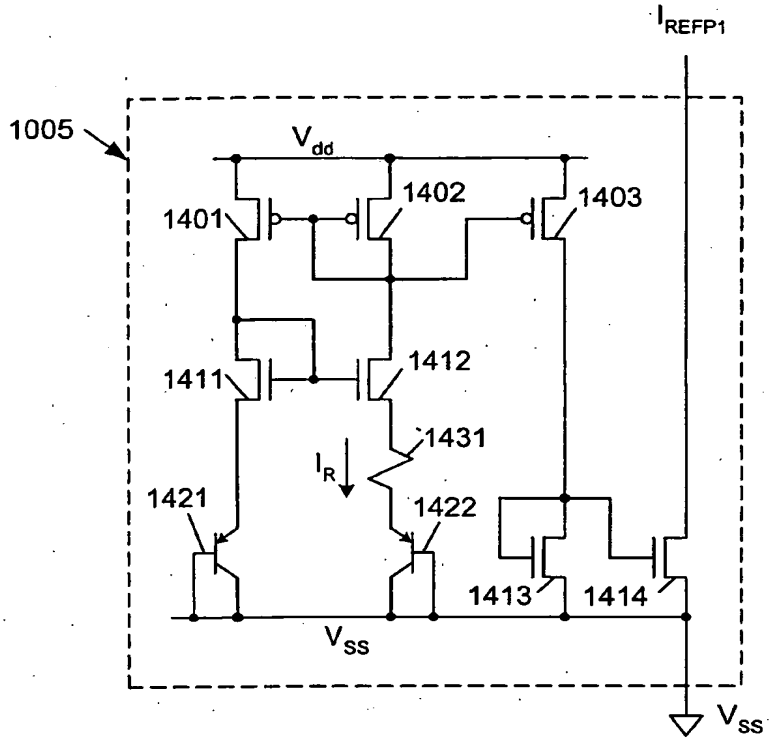

I_REFP1
1005
V_dd
1401
1402
1403
1411
1412
1431
I_R
1421
1422
1413
1414
V_SS
V_SS

FIG. 14

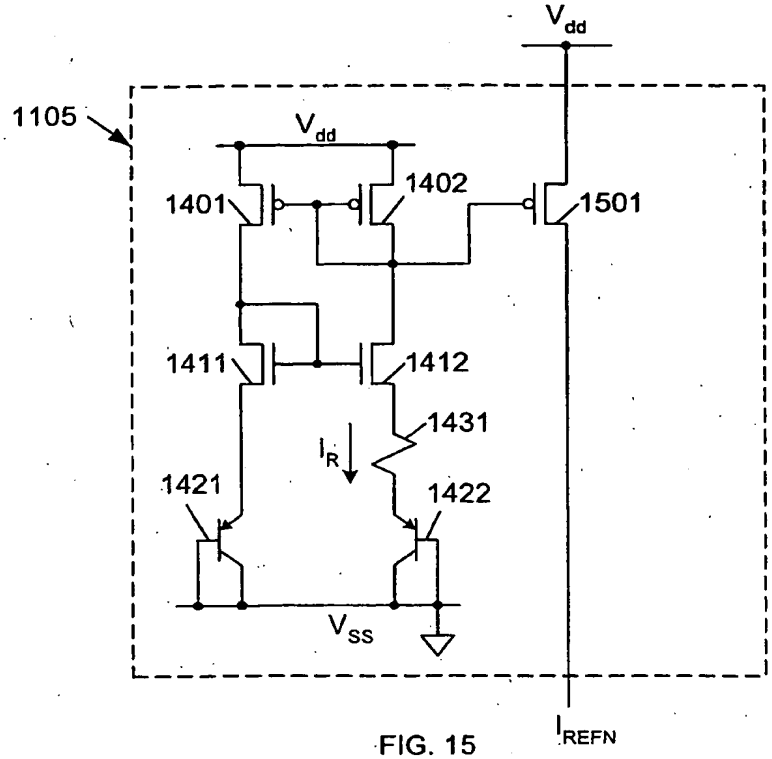

V_dd
1105
V_dd
1401
1402
1501
1411
1412
1431
I_R
1421
1422
V_SS
I_REFN

FIG. 15

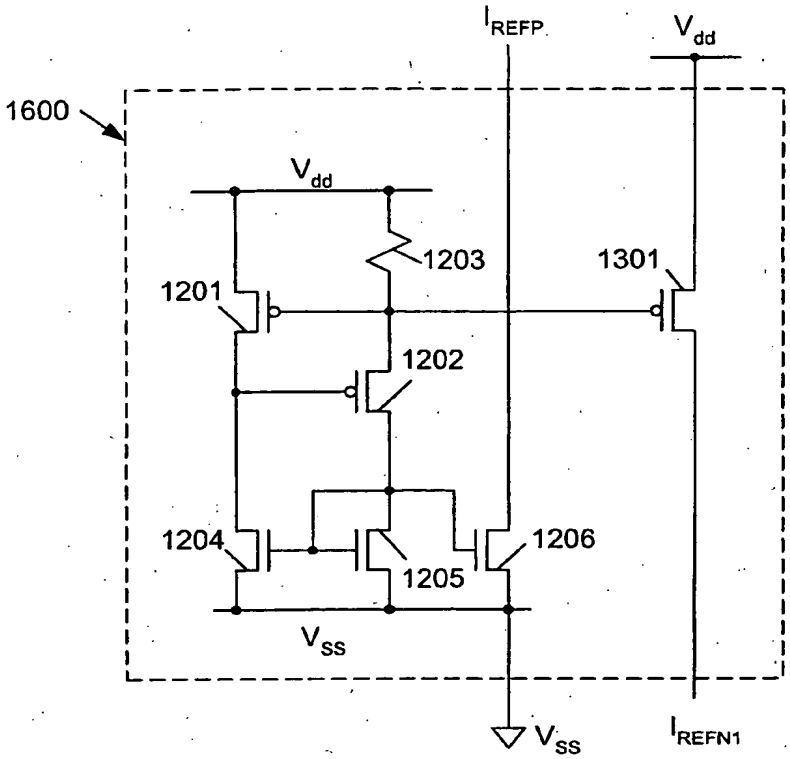

I_{REFP}
V_{dd}
1600
V_{dd}
1203
1301
1201
1202
1204
1205
1206
V_{SS}
V_{SS}
I_{REFN1}

FIG. 16

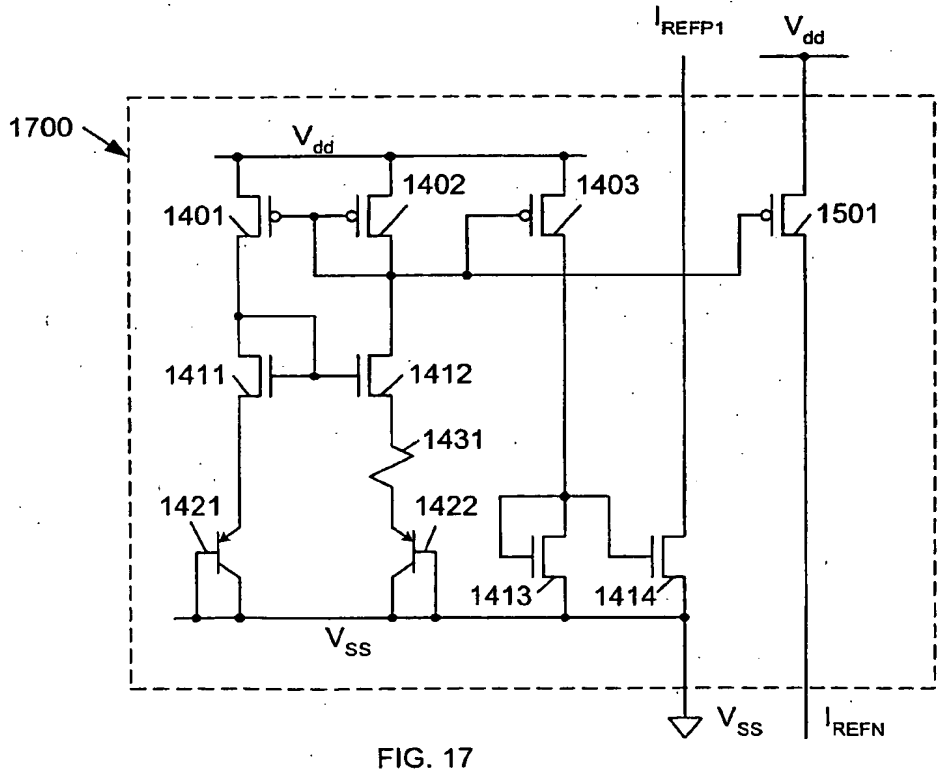

I_{REFP1}
V_{dd}
1700
V_{dd}
1402
1403
1401
1501
1411
1412
1431
1421
1422
1413
1414
V_{SS}
V_{SS}
I_{REFN}

FIG. 17

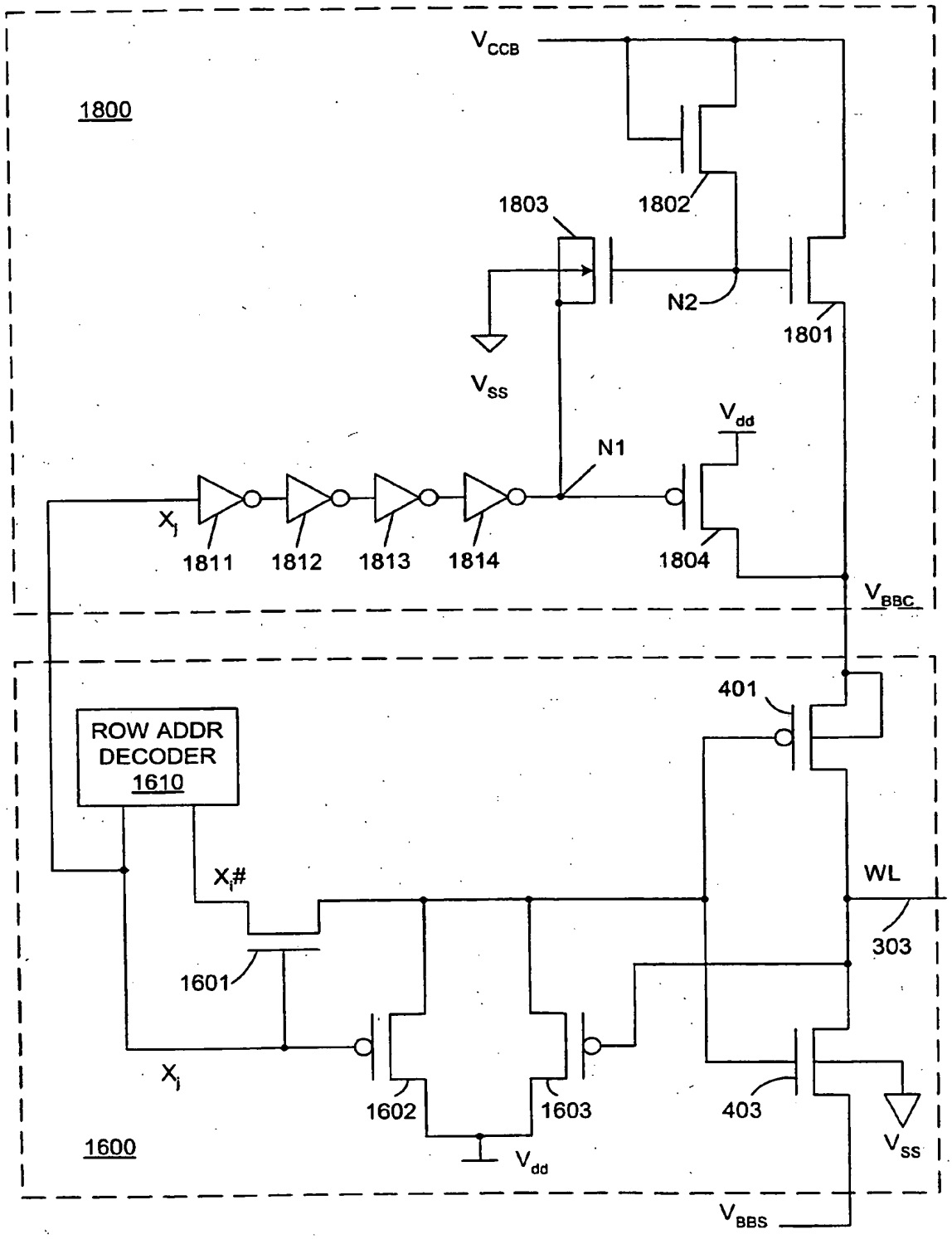

1800
V_{CCB}
1803
1802
N2
1801
V_{SS}
V_{dd}
N1
X_j
1811
1812
1813
1814
1804
V_{BBC}
401
ROW ADDR DECODER 1610
X_j#
WL
303
1601
X_j
1602
1603
403
V_{SS}
1600
V_{dd}
V_{BBS}

FIG. 18

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 99/18536

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C5/14 G11C8/00 G11C11/408

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 493 659 A (IBM) 8 July 1992 (1992-07-08) the whole document	1
A	EP 0 632 462 A (IBM) 4 January 1995 (1995-01-04) the whole document	1
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 07, 31 July 1996 (1996-07-31) & JP 08 063964 A (MITSUBISHI ELECTRIC CORP), 8 March 1996 (1996-03-08) abstract	11

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 December 1999	11/01/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Degraeve, L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/18536

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 460 694 A (NIPPON ELECTRIC CO) 11 December 1991 (1991-12-11) column 7, line 53 -column 14, line 32; figures 5,6	11
A	US 5 297 104 A (NAKASHIMA TAKASHI) 22 March 1994 (1994-03-22) the whole document	1

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

In ational Application No
PCT/US 99/18536

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0493659 A	08-07-1992	US 5075571 A	24-12-1991
		DE 69126292 D	03-07-1997
		DE 69126292 T	11-12-1997
		JP 2103131 C	22-10-1996
		JP 6209090 A	26-07-1994
		JP 8017226 B	21-02-1996
EP 0632462 A	04-01-1995	JP 2731701 B	25-03-1998
		JP 7065573 A	10-03-1995
		US 5504702 A	02-04-1996
JP 08063964 A	08-03-1996	NONE	
EP 0460694 A	11-12-1991	JP 4042494 A	13-02-1992
		DE 69130589 D	21-01-1999
		DE 69130589 T	15-07-1999
		KR 9509230 B	18-08-1995
		US 5287325 A	15-02-1994
US 5297104 A	22-03-1994	KR 9402859 B	04-04-1994
		JP 2662335 B	08-10-1997
		JP 5089673 A	09-04-1993